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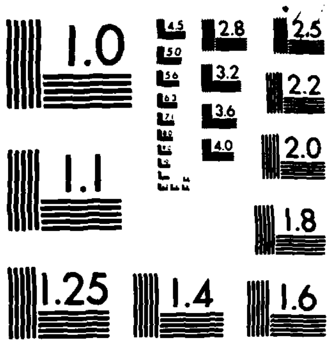

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EXPERIMENTAL INVESTIGATION OF
SWITCHED-CAPACITOR CIRCUITS
AND SYSTEMS

THESIS

AFIT/GE/83D-60

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EXPERIMENTAL INVESTIGATION OF SWITCHED-CAPACITOR CIRCUITS AND SYSTEMS

THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology,

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

by

Dundar Satirtav

1st Lt.

TURKISH AIR FORCE

Graduate Electrical Engineering

December 1983

PREFACE

Replacement of certain analog elements)y their switched-capacitor equivalents is a relatively new technology with potential applications in integrated circuit design. The first investigations on this techniquie was performed in the late 1970's and attracted great deal of attention. One of the important reasons for replacing analog circuits with their switched-capacitor equivalents is the compatibility of the switched-capacitor circuits with MOS technology. Present emphasis is directed toward switched-capacitor realization of the entire analog sampled data systems in MOS technology.

The purpose of this experimental research was to investigate certain switched-capacitor circuits in order to verify their theoretical analysis.

I greatfully acknowledge the support and technical advise of Captain Russell W. Hensley and First Lieutenant Keith R. Jones.

My appreciation is extended to Mr. Bob Durham for his assistance in acquiring me with necessary equipment for my experiment.

For their interest and for their patience I thank my committee members Dr. V. Syed and Lt. Col. J. Carnaghie.

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And finally, I express my frofound gratitude to my family in Turkey, and my girlfriend Pamela S. Davie for their continuous encouragement.

Dundar Satirtav

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ABSTRACT

In the literature , there are many technical papers describing the theoretical characteristics, advantages and disadvantages of switched-capacitor circuits and systems. The experimental resarch presented here is an investigation of the characteristics of specific switched-capacitor circuits as described by some of these technical papers. The circuits investigated include a second order band elimination filter, a simulation of inductor and a AM demodulator. For each circuit, the performance of the switched-capacitor implementation was compared to the theoretical analysis. In additon, for the band elimination filter and inductor circuits, the performance of the switched-capacitor circuit was compared to an equivalent implementation using normal analog components. Analatical results were duplicated using switched-capacitor circuits. The clock frequency was a critical parameter for the experiment.

CHAPTER I

INTRODUCTION

BACKGROUND

The main building block of active filters is the integrator which consists of operational amplifier (op-amp), resistor and capacitors. A maj· :eason that active filters have not previously been integr ..ed in MOS technology is the necessity to accurately de : · resistance-capacitance products, which requires that the absolute value of the resistors and capacitors be well controlled. In addition, integrated (diffused) resistors have poor temperature and linearity characteristics, as well as, requiring a large amount of silicon area. A circuit that performs the function of a resistor without these disadvantages has been investigated independently by several workers. That circuit is the switched-capacitor(SC) circuit.

The fundamental of a characteristic SC circuit is the transferral of charge from point to point in the circuit by charging a capacitor at the first point and discharging it through the other. The theory of the operation of a SC circuit as a resistor has been explained in detail in Appendix A. If the switching rate, $f_c = 1/T_c$, is much larger than the highest frequency of the signal of interest, then the discontinuities of the signal can be ignored and the SC can then be considered as a direct replacement for a conventional resistor. However if, the switching rate is of the same order as the highest signal frequency, then analysis must incorporate sampled data techniques. As for any sampled data system,the input signal should be band limited below $\frac{f_c}{2}$ as dictated by the sampling theorem. The stability and linearity of the resistance value (Eq. A-4) is much better than that obtained from diffused resistors since the insulator in a properly fabricated MOS capacitor has essentialy ideal characteristics. For example, typical temperature coefficients for these capacitors are less than 10 ppm (Ref 2:601). Another important advantage of the SC resistors is the high accuracy of the RC time constant that can be obtained with their use.

In integrated circuits, it is possible to achieve high precision in the capacitance ratio. It has been shown that, the error in such ratios can be less than 0,1 percent using standard MOS techniques (Ref 3:371-379). It is thus apparent that the SC resistor makes it possible to design precise, stable RC filters which can be fully integrated. It is also possible to modify the filter parameters such as, gain, cutoff frequency and selectivity by varying either the SC clock frequency or the capacitor values or both.

Experimental investigations (Ref 2;4) show that the effects of the switches and amplifier limitations must be taken into account as practical design considerations. Some of these limitations are following:

1. It is desirable to have the clock rate as high as possible relative to the filter bandpass frequencies in order to reduce the aliasing of the input signal. The magnitude of the capacitor ratios required for a given frequency response increases with the clock rate, which also increases the silicon area requirements.

2. At very high sampling rates, the time constant of the switched capacitors will become important.

3. Due to finite ON resistance of the switches, the transfer of the charge is incomplete.

4. The thermal noise contributions of the amplifier and switches dominate over all other noise sources.

5. There is clock feedthrough which is caused by the inherent capacitance between diffusion and gate of the switching transistors.

6. The offset error caused by leakage current in the switching capacitor between sampling period is an important parameter.

7. There is stray capacitance between the capacitor electrode and ground. The stray capacitances upset the symmetry of the circuit and hence introduce additional image frequencies.

There are investigations underway to preserve the well known low sensitivity properties of doubly loaded ladders (analog reactance filters :ARF) in SC filters. One of the most promising approaches consists of replacing all branches of the ARF by equivalent branches in a SC filter (Ref 5).

Generally many of the SC networks described in the literature have been either for filtering or for analog to digital conversion applications. The SC building blocks are also useful for realizing many other signal processing functions. Another application of the SC building blocks is the realization of the adaptive systems. The paper by Martin and Sedra (Ref 7) gives design examples of a SC phase lock loop, a tracking filter, a programmable equalizer, a quadrature sinusoidal generator, and an adaptive channel equalizer using SC networks. Still another important example is a SC realization of a spectral line enhancer (Ref 8). This is an adaptive system which tracks the peak of the spectral density function of the input signal. These examples are strong evidence for the important role which SC networks can be expected to play in VLSI implementation of signal processing functions.

A recent trend in SC filter design is to eliminate the use of op-amps which form the basic integrators or to reduce the number of op-amps by multiplexing them (Ref 9). Op-amps require a large chip area, and consume large amounts of power. The bandwidth of the filter will also improve if op-amps can be avoided. Other advantages of elimination of the op-amps include reduced noise and improved dynamic range. Jamal and Holmes presented a novel tecnique to avoid the use of the op-amps to form the basic integrator enhancement type NMOS transistors and MOS capacitors (Ref 10).

STATEMENT OF THE PROBLEM AND SCOPE

The objective of this research work is to analyze and verify in the lab various SC circuits and systems (second order SC band elimination filter, SC simulation of an inductor, and SC synchronous demodulator). This work was accomplished in two phases :

I. Examination of a technical paper that analyzes a particular system using SC circuits. This paper claims certain performance attributes, advantages, and disadvantages.

II. Actually building and testing the circuit or the system, and investigating whether it really performs as indicated. If it does, explain why, and if it does not explain why not.

ASSUMPTIONS

For experimental purposes

I. Input signals are changing very slowly in time with respect to the two phase clock.

II. The capacitor appears to charge instantaneously to the input voltage.

III. The period of the capacitor discharge (T=RC) is very much less than the reciprocal of the input signal bandwidth. Thus, the capacitor appears to discharge instantaneously.

IV. Equipment used have good temperature characteristics so that experimental measurments do not change as time elapses.

The second and third assumptions refer to ideal switches. The ideal switch assumption is quite reasonable if the signals of interest are varying slowly with time.

For computational purposes

I. Voltage sources have zero resistance.

II. Operational amplifiers are ideal (infinite gain).

III. Switches have zero ON resistance so that complete transfer of charge can be accomplished.

APPROACH AND PRESENTATION

Each chapter represents a different phase of this experimental research. Chapter II presents analysis, design, fabrication, and test of the second order SC bandelimination filter for a given transfer function. It includes effects of changes in clock frequency, effect of stray capacitance and clocking scheme on filter performance.

Chapter III presents simulation of grounded and floating inductors using SC circuits. This section justifies the equivalance of the proposed SC inductor to grounded inductor. A test circuit built using SC circuits in place of resistors and a grounded inductor is given. The test circuit is a resonant circuit. The performance of the test circuit is compared with an analog resonant circuit. Another test circuit, showing the operation of the floating inductor, is also presented.

Chapter IV addresses the realization of SC synchronous demodulator. The results are illustrated in the chapter.

Chapter V draws conclusions about the experiments conducted, and recommends further research in different application areas of SC circuits.

Equally important is the information contained in Appendix A, Appendix B, and Appendix C. They present basic principles of operation of the SC circuit as a resistor, two phase clock circuit, and the sampled data demodulation technique respectively.

CHAPTER II

SECOND ORDER SC FILTER

ANALYSIS AND DESIGN

There are several general approaches for the design of switched-capacitor (SC) filters. Conceptually ,the simplest approach is to first obtain the analog circuit and then replace the resistors by their equivalent switched-capacitors.

The filter realized is a second order SC band-elimination filter. Its transfer function is

$$H(s) = \frac{(s + 1000)\ (s + 5000)}{(s + 500)\ (s + 10000)} \qquad (2 - 1)$$

The analog filter that satisfies this specification is shown in Figure II-1.

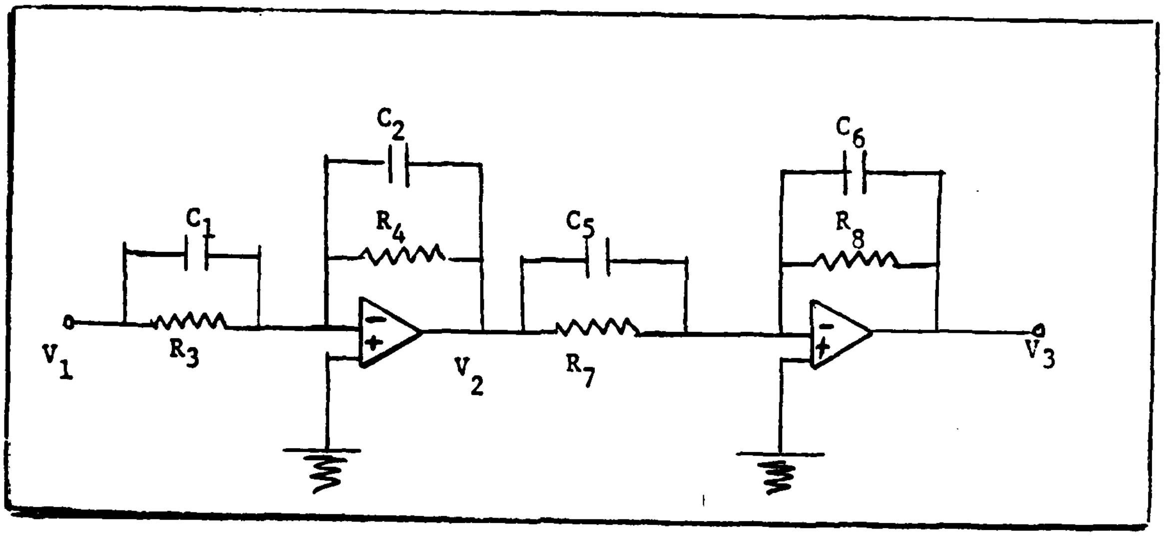

Figure II-1 Second order analog filter

This is the cascaded form of the two first order filters. The transfer function of the first order part is

$$H(s) = \frac{v_2}{v_1} = \frac{Z_2}{Z_1} = \frac{C_2//R_4}{C_1//R_3} \qquad (2 - 2a)$$

which can be simplified to the following equation

$$H(s) = - \frac{C_1}{C_2} \frac{s + 1/R_3C_1}{s + 1/R_4C_2} \qquad (2 - 2b)$$

R_3 can be replaced by $\frac{1}{f_cC_3}$ and R_4 can be replaced by $\frac{1}{f_cC_4}$ where f_c is two phase non-overlaping clock frequency (see Appendix B). Then, the corresponding equation for the SC is

$$H(s) = - \frac{C_1}{C_2} \frac{s + f_c\ (C_3/C_1)}{s + f_c\ (C_4/C_2)} \qquad (2 - 3)$$

The product H(s) can be factored into the form of Eq. 2-1. Then,

$$H(s) = \frac{s + 1000}{s + 500} \frac{s + 5000}{s + 10000} \qquad (2 - 4)$$

The coefficient of Eq. 2-4 are equated with those of Eq. 2-3. For convenience $C_1 = C_2$, therefore, $\frac{C_1}{C_2} = 1$. Depending on the clock frequency choosen, the values of C_3 and C_4 can be found.

If the resistors are replaced with SC, the circuit depicted by Figure II-1 becomes Figure II-2 (Ref 1:420).

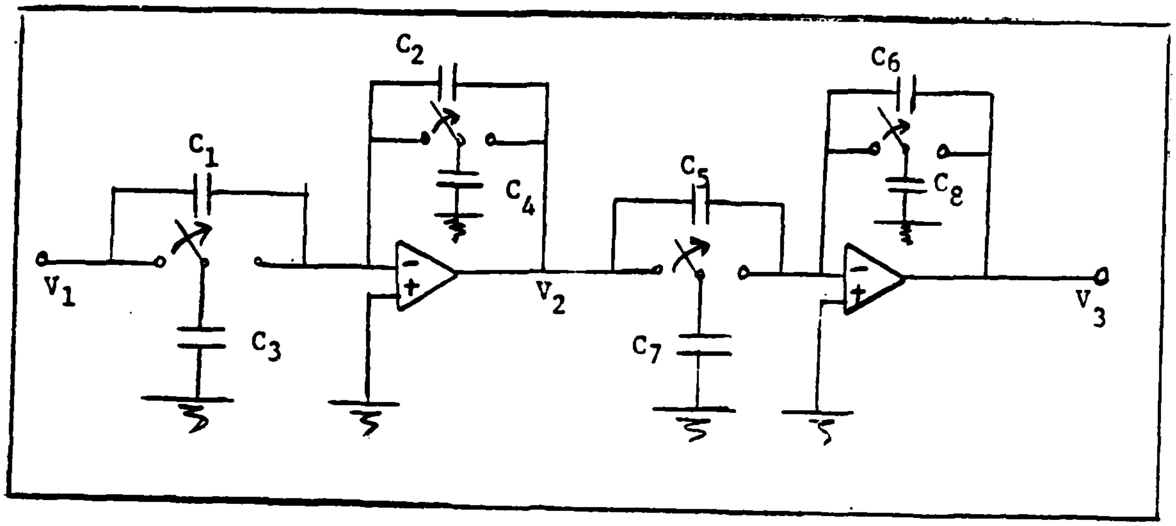

Figure II-2 SC equivalent of Figure II-1

The same procedure can be followed to realize the second order part of the SC filter. As mentioned before, the direct replacement of resistors with switched-capacitors requires that **the switching frequency must be much larger than the significant spectrum frequencies of the input signal** (Ref 1:409). The clock that will be used throughout the experiment was developed in Appendix B.

FABRICATION AND TEST

For comparison purposes, the analog filter and its equivalent SC filter were built. The operational amplifiers used were SN72741 and SN72747. The analog switches used were type DG201A. DG201A is a SPST (Single Pole Single Throw) switch. Characteristics and pin description of the chips used are in Appendix D. The experiment was conducted for clock frequencies of 5 Khz, 50 Khz, 100 Khz and 200 Khz. For convenience, C_1, C_2, C_5, and C_6 are choosen to be 0,1µF. The values of C_3, C_4, C_7 and C_8 were computed by equating Eq. 2-3 and Eq. 2-4. Table II-1 shows the corresponding values of these capacitors for each clock frequency. The capacitances were measured using an 820 Capacitance Meter by BK Precision Dynascan Corporation.

Table II-1

Element values

Clock Fr.	C_1,C_2,C_5,C_6	C_3	C_4	C_7	C_8
50Khz	0,1 µF	$2*10^3$ pF	1000 pF	0,01 µF	0,02 µF
100Khz	0,1 µF	1000 pF	500 pF	$5*10^3$ pF	0,01 µF
200Khz	0,1 µF	500 pF	250 pF	2500 pF	$5*10^3$ pF

The SC filter resistor equivalences of the analog filter were 10, 20, 2, and 1 Kilo ohm for R_3, R_4, R_7 and R_8 respectively.

Effect of change in clock frequency

The first experiment was conducted for 5 Khz clock frequency. Since the clock frequency was small, the output of the op-amp did not remain constant. The output of op-amp followed the slow clock pulses.

Even though the clock frequency was small, the first order output waveform of the digital filter was the same as the analog filter output. However, the switching action was observed on the output of the first order part of digital filter. The output waveform of the second order part of the digital filter did not resemble the output signal of the analog filter. Figure II-3 shows the typical output waveform of the first order part of the digital filter for 5 Khz clock frequency. The input signal frequency is 550 Hz.

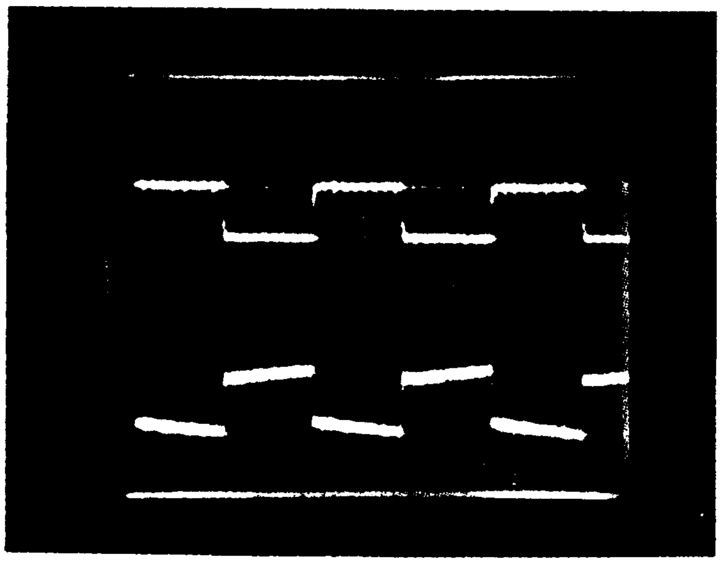

Figure II-3 Input (top trace)- output relationship of the first order SC filter for 5 Khz clock frequency.
Horizontal: 0.5 ms/div
Vertical: 1 V/div

Later, the experiment was conducted with clock frequencies of 50 Khz, 100 Khz and 200 Khz. As the clock frequency is increased, switching action on the output signal disappears, and the thermal noise due to the op-amps and switches decreases. By comparing Figures II-4 and II-5, the reasons for this change becomes apparent. Figure II-4 shows both the input (top trace) and the output (bottom trace) of the analog filter. Figure II-5 shows the output of the SC equivalent filter. The clock frequency is 100 Khz. Comparing the two figures, the digital output is almost identical to analog output.

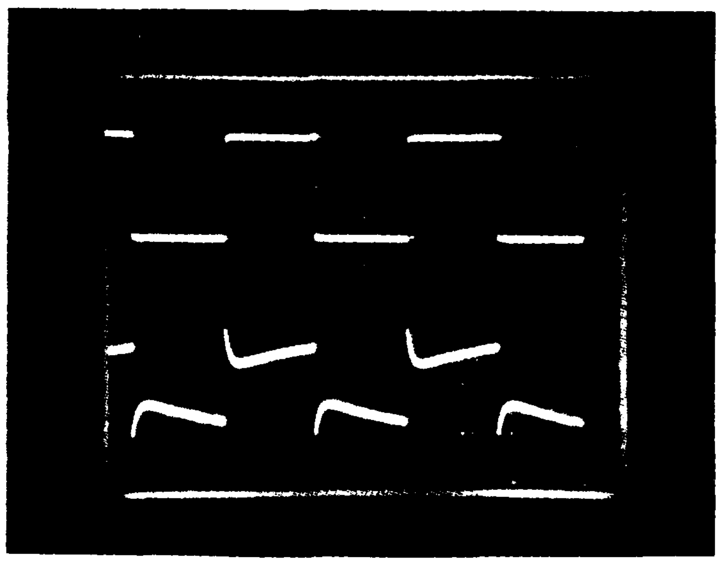

Figure II-4 Second order analog filter
Input (top trace) - output
Horizontal: 1 ms/div
Vertical: 0.5 V/div

But, as it was mentioned in the introduction section, the sizes of the capacitance ratios for a given frequency response also increases with the clock frequency, which increases silicon area requirements. The minimum clock frequency is determined by the time constant of the switched capacitors and by the slew-rate and bandwidth limitations of the amplifiers used in the SC circuit. The minimum clock frequency is limited by Nyquist's sampling rate and by considering dissipative losses in the MOS capacitors. These dissipative losses result in a loss of charge. It must also, be taken into account that any dielectric gradients may degrade the matching of too large capacitors. The selection of the minimum size of a MOS capacitor should be governed by considering paracitic capacitances and noise contribution due to the thermal noise of the switches.

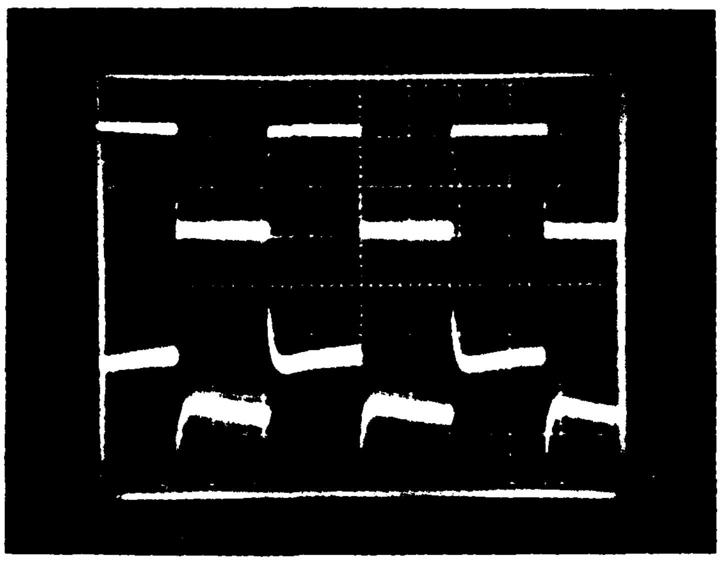

Figure II-5. Second order SC filter (Input versus Output)

This r.m.s noise is given by (kT/C), where C is the switched-capacitor and the kT is the thermal voltage (Ref 11:76). Figure II-6 shows the effect of the clock frequency on the output signal.

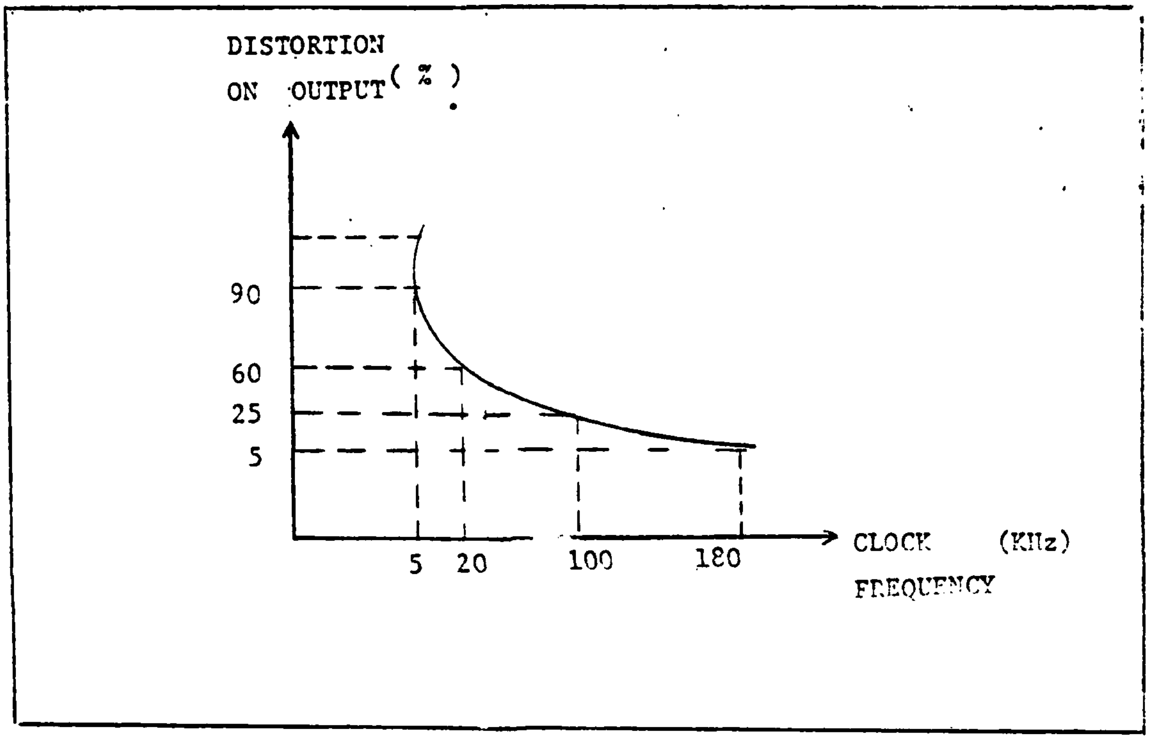

Figure II-6 Clock frequency versus distortion on output

As it is seen from Eqs. 2-3 and 2-4, the filter bandwidth can be adjusted by either changing the clock frequency or the capacitor ratios. This situation was observed for different clock frequencies and different capacitor ratios. Figure II-7 shows the frequency response of the SC filter realizing Eq. 2-1 for the clock frequency of 100 Khz.

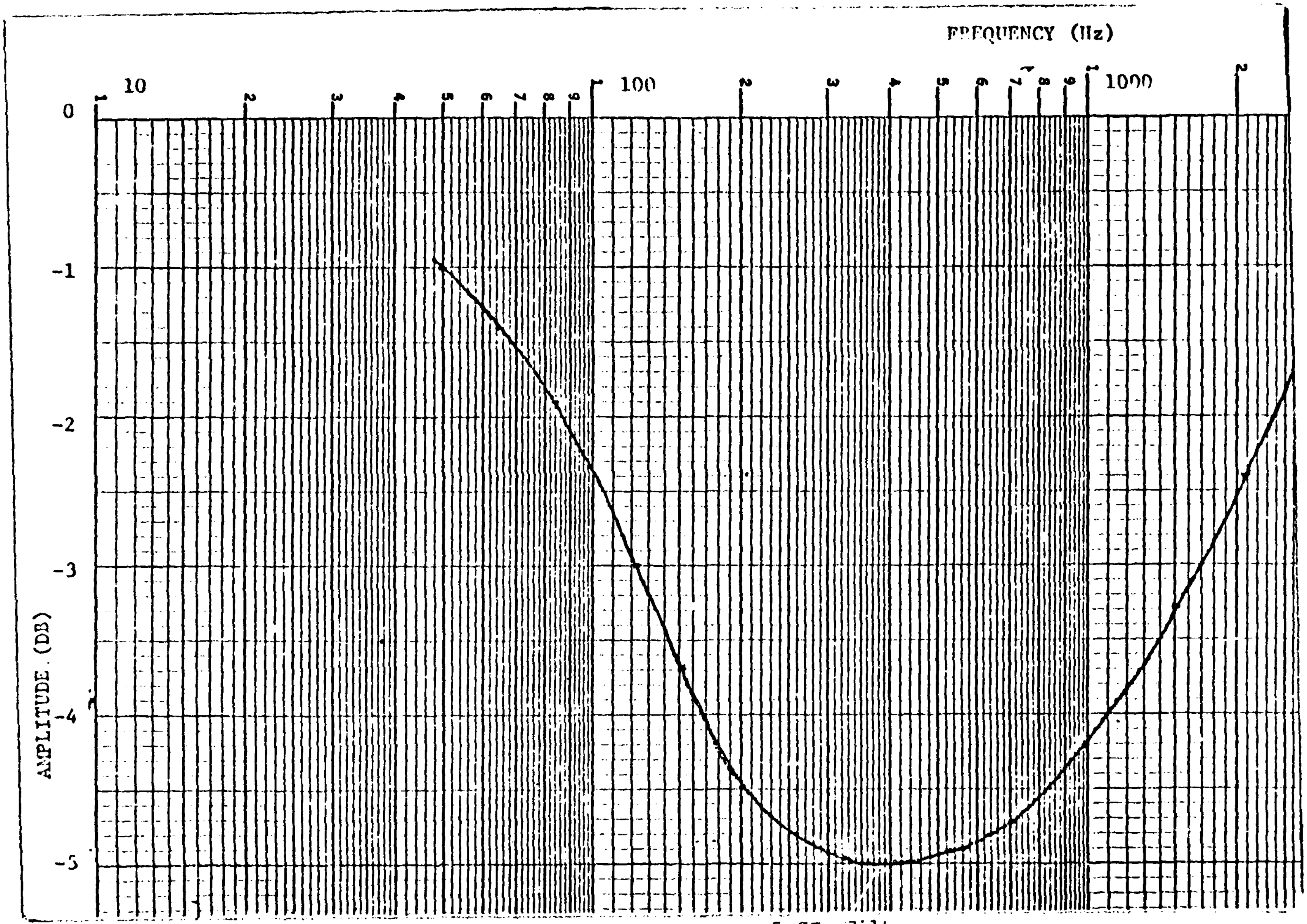

Figure II - 7 Frequency Responce of SC Filter.

Effect of different clocking schemes

The experiment was conducted using two different clocking schemes. The first scheme was such that all switched capacitors were clocked in phase while the second was such that every other switched-capacitor was clocked 180° out of phase, as illustrated in Figure II-8.

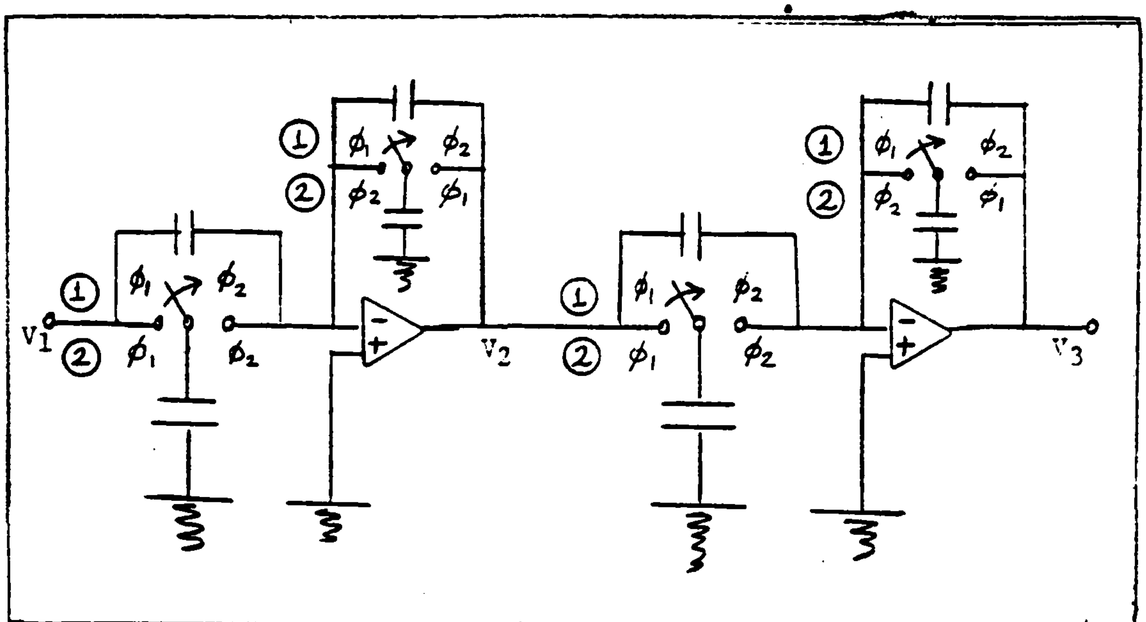

Figure II-8 Two different clocking schemes for SC filter.

The results of the experiment indicated that there was no significant change in the magnitude response due to the use of different clocking schemes. However, the output signal of the filter using the first clocking scheme was distorted.

Two pictures were taken to illustrate the effects of the two different clocking schemes. Figure II-5 shows input output relationship for the first clocking scheme and

Figure II-9 for the second clocking scheme. The top trace shows input signal and the bottom trace shows output of the filter. There is more noise on the output signal of Figure II-5 as indicated earlier.

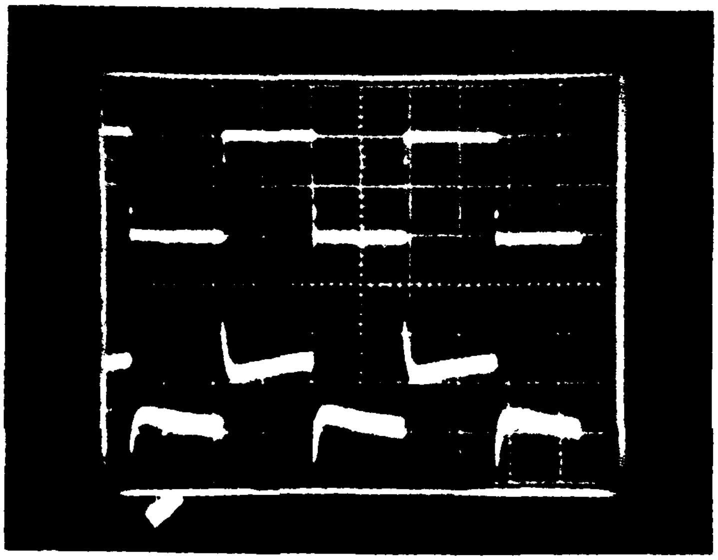

Figure II- 9 Input-output relatioship of SC filter using the second clocking scheme.

Effect of stray capacitance

Any floating capacitor (C) of an SC filter gives rise to stray capacitances between the capacitor electrodes and ground. As illustrated in Figure II-10 the capacitance C_1 from the bottom electrode to ground is typically between 5 to 20 percent of the main capacitance C . The capacitance C_2 from the top electrode to ground is between 0,1 to 1 percent of the C . To eliminate the effects of the stray capacitances the bottom electrodes of all capacitors should be connected to a voltage source or a real or virtual ground (Ref 6). The experiment was conducted with all capacitors grounded to prevent any degradation in the filter realization due to stray capacitance effects.

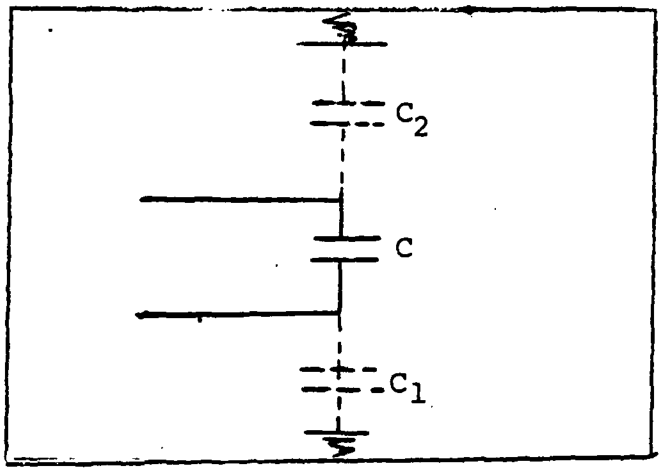

Figure II-10 Stray capacitance

CHAPTER III

SWITCH-CAPACITOR SIMULATION OF INDUCTOR

ANALYSIS AND DESIGN

The recent interest in the design of SC networks has been motivated by the goal of realizing an active filter on a chip. Most efforts have been directed to the realization of resistors connected to capacitors, by SC combinations. A challenging question that comes to mind is whether inductors can also be simulated by active SC combinations.

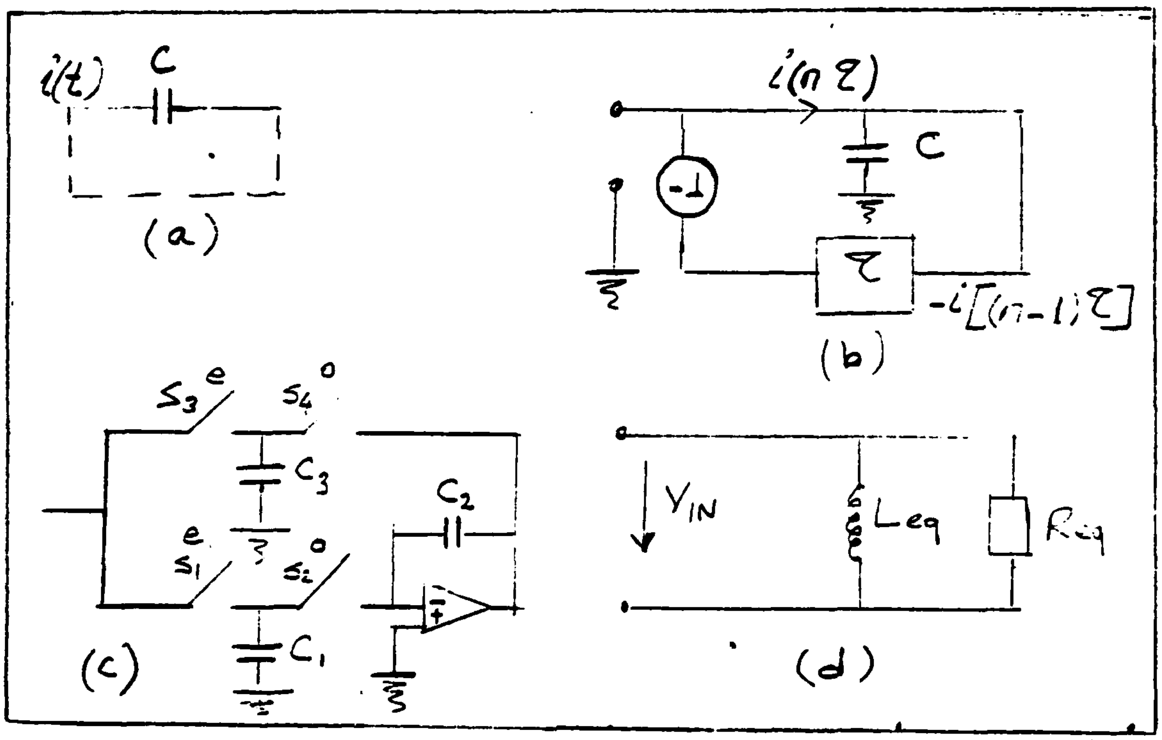

Figure III-1 a) a capacitor b)principle of obtaining SC inductor c) SC inductor d) equivalent circiut of (c)

Consider the capacitor C shown in Figure III-1a, the incremental charge $q(t)$ stored at any time t can be expressed in terms of the current $i(t)$ and the voltage $v(t)$:

$$q(t) = \int_0^t i(t)dt = C\,v(t) - C\,v(0) \qquad (3 - 1)$$

where $v(0)$ represents the voltage across the capacitor at time $t=0$. Assuming now that the capacitor is not charged continuously but in surges of $i(n\tau)\ (t-n\tau)\,\tau_0$, after every interval τ, where τ_0 is a unity time constant that is required to maintain the proper dimensions in the charge equation, and $(t-n\tau)$ is the Kronecher delta sequence, then it can be shown that (Ref 10:77) the nodal charge equation is given by

$$i(t) = \frac{C}{\tau_0}\,[v(t) - v(t - \tau)] \qquad (3 - 2)$$

Consider the relation between current i and voltage v for the capacitor C shown in Figure III-1a is

$$i(t) = C\,\frac{dv(t)}{dt} \qquad (3 - 3)$$

If the capacitor is assumed to be a discrete-time system and the sampling period τ is much smaller than the signal period, it can be assumed that the current does not change during τ . Hence it is possible to replace the continuous-time derivative in Eq. 3-3 by a finite-difference form of the derivative; i.e at time $t = n\tau$, the current is

$$i(n\tau) = C \frac{v(n\tau) - v[(n-1)\tau]}{\tau} \qquad (3-4)$$

where $v(n\tau)$ and $v[(n-1)\tau]$ are two adjacent time samples of the voltage.

By similar reasoning it readily follows that the charge equation for an inductor is given by

$$v(t) = \frac{L}{\tau_o}[i(t) - i(t - \tau)] \qquad (3-5)$$

This can be simulated using switched-capacitors (Ref 12) if we can obtain a building block that yields the equation

$$v(t) = \frac{\tau_o}{C}[i(t) - i(t - \tau)] \qquad (3-6)$$

in this case the equivalent inductor has the value

$$L_{eq} = \frac{\tau_o^2}{C} \qquad (3-7)$$

with $t = n\tau$, the difference equation of Eq. 3-6 corresponds to the configuration given by Figure III-1b. This configuration can be realized by the active network shown in Figure III-1c (Ref 12). The switches s^e and are closed during even and odd times n respectively.

In Figure III-1c the capacitor C_1 stores the charge $C_1 v_{in}(n)$ and converts it into a current which is delayed and inverted at C_2 . The capacitor C_3 then integrates the difference between the direct and the delayed current component according to the nodal charge equation given by Eq. 3-6.

The equivalent circuit of Figure III-1c can be obtained as in Figure III-1d. The analysis is similar to that of RC equivalent of an inductor. RC equivalent of Figure III-1c is as in Figure III-2.

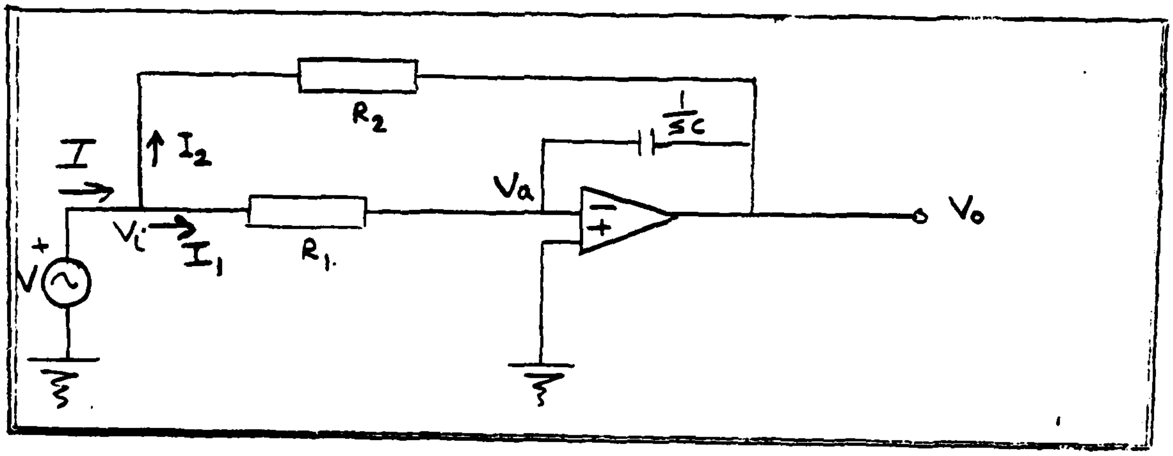

Figure III-2 RC inductor.

On Figure III-2

$$Z_{in} = \frac{v_i}{I} \qquad (3 - 8)$$

the current balance at node is

$$I = I_1 + I_2 \qquad (3 - 9)$$

where

$$I_1 = \frac{v_i - v_a}{R_1} = \frac{v_i}{R_1} \qquad (3 - 10)$$

$$I_2 = \frac{v_i - v_o}{R_2} \qquad (3 - 11)$$

therefore,

$$I = \frac{v_i}{R_1} + \frac{v_i - v_o}{R_2} \qquad (3 - 12)$$

and

$$v_o = v_i \frac{-1}{R_1 CS} \qquad (3 - 13)$$

so

$$I = \frac{v_i}{R_1} + \frac{v_i}{R_2} + \frac{v_i}{R_2}\left(\frac{1}{R_1 CS}\right)$$

$$= v_i\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_1 R_2 CS}\right) \qquad (3 - 14)$$

and

$$Z_i = \frac{R_1 R_2 CS}{1 + R_1 CS + R_2 CS} = \frac{R_1 R_2 CS}{1 + (R_1 + R_2)CS} \qquad (3 - 15)$$

Z_i for the circuit in Figure III-1d is

$$Z_i = \frac{sL_{eg}}{1 + sL_{eg}/R_{eg}} \qquad (3 - 16)$$

Equating Eqs.3-15 and 3-16, we get

$$R_1R_2C = L \qquad \text{and} \qquad (R_1 \;\; R_2)\; C = L/R$$

from these $\quad L_{eg} = R_1R_2C \qquad (3 - 17)$

$$R_{eg} = R_1 \;//\; R_2 \qquad (3 - 18)$$

If R_1 is replaced by $\dfrac{\tau_o}{C_1}$, R_2 by $\dfrac{\tau_o}{C_3}$ and C by C_2

then

$$L_{eg} = \frac{\tau_o^2}{C_1C_3} C_2 \qquad (3 - 19)$$

and

$$R_{eg} = \frac{\tau_o}{C_1 + C_3 - C_1C_3/C_2} \qquad (3 - 20)$$

FABRICATION AND TEST

A SC resonant circuit was built by replacing inductor and resistor with their equivalent SC circuits (Ref 12). The SC circuit (Figure III-3) was designed using DG181 SPST (Single pole single throw) switches, SN72741 op-amp, and capacitors whose values are shown in Table III-1. Based upon these values and Eqs. 3-17,18, the SC resonant circuit simulated a series resistor of 28749 ohms, a parallel inductor of 11.2 mH, a parallel capacitor of 2.579 μF and a parallel resistor of 3157 ohms.

Table III-1

Capacitor values for SC circuit

Capacitors	Capacitances
C	2.579 μF
C_0	2.174 nF
C_I	10.4 nF
C_2	0.28 nF
C_3	9.4 nF

The pin description and electrical characteristics of these chips are listed in Appendix D. The experiment was conducted at a clock frequency of 16 Khz.

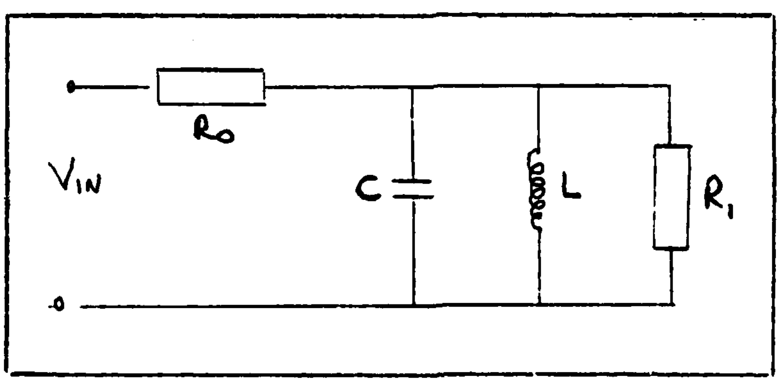

Figure III-3 Analog resonant circuit

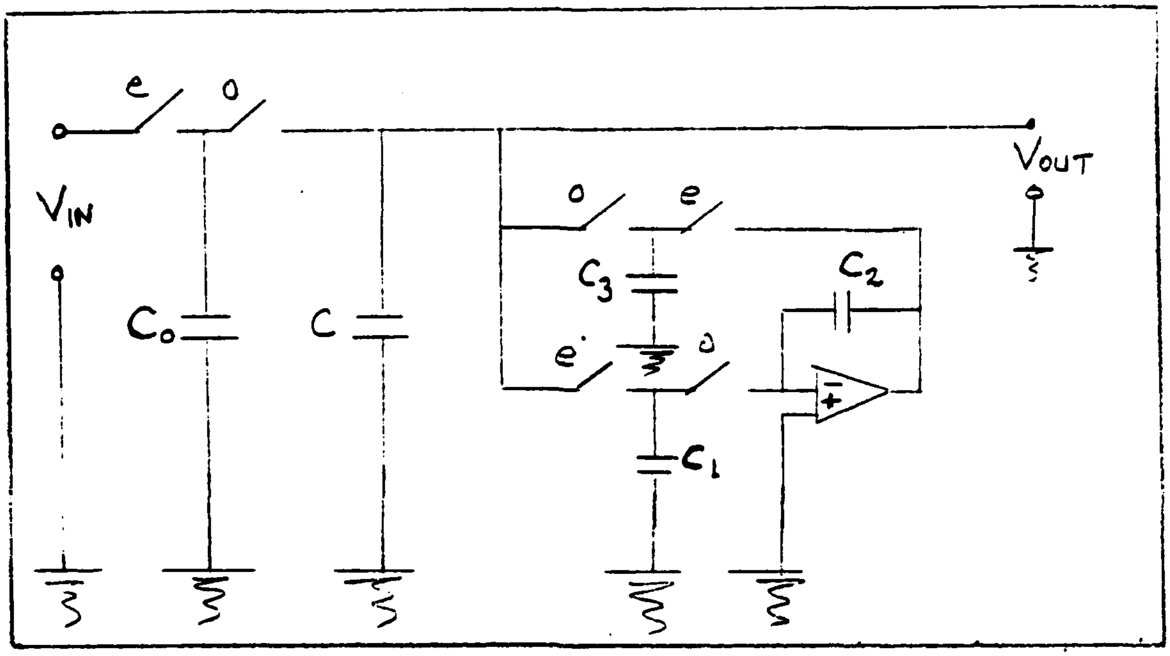

Figure III-4 SC resonant circuit

The observed frequency responce (Figure III-5) of the SC circiut had a sharp peak at 1050 Hz and half power point at 1000 Hz and 1100 Hz. Figure III-6 shows the theoretical frequency response of the corresponding analog resonant circuit. Overlooking the small discrepancy at resonant frequency, there is agreement between the frequency responses of the SC circuit and corresponding analog circuit. This dicrepancy is due to the parasitic capacitances introduced by the discrete components and non-ideal characteristics of the SC circuit elements.

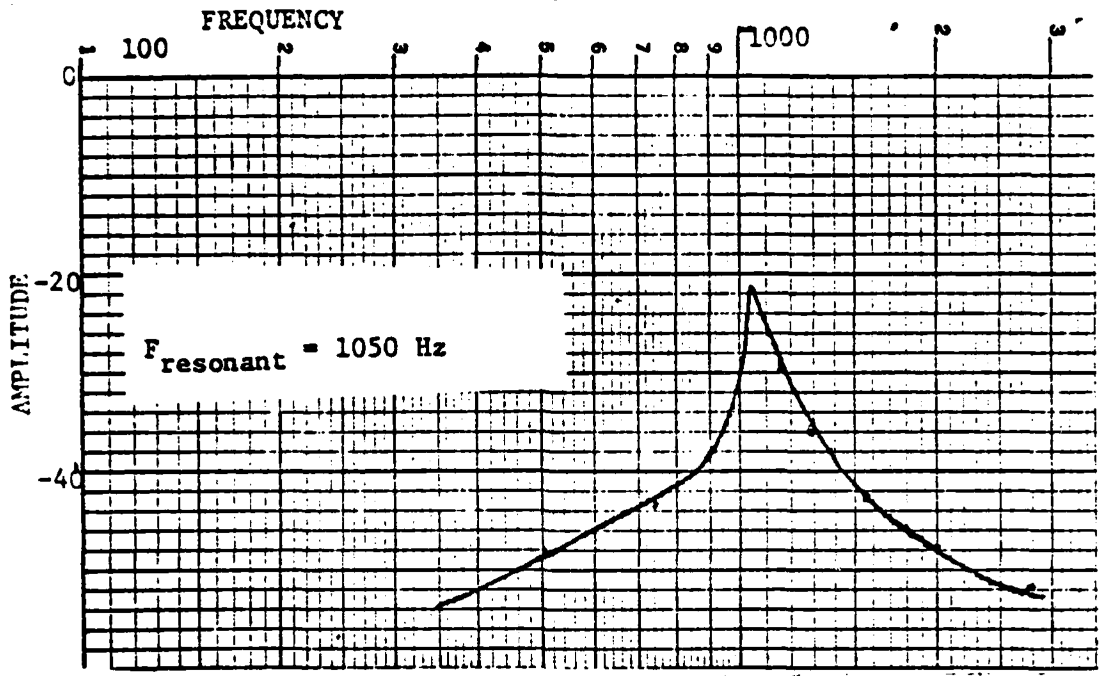

Figure III-5 Frequency response of SC resonant circuit

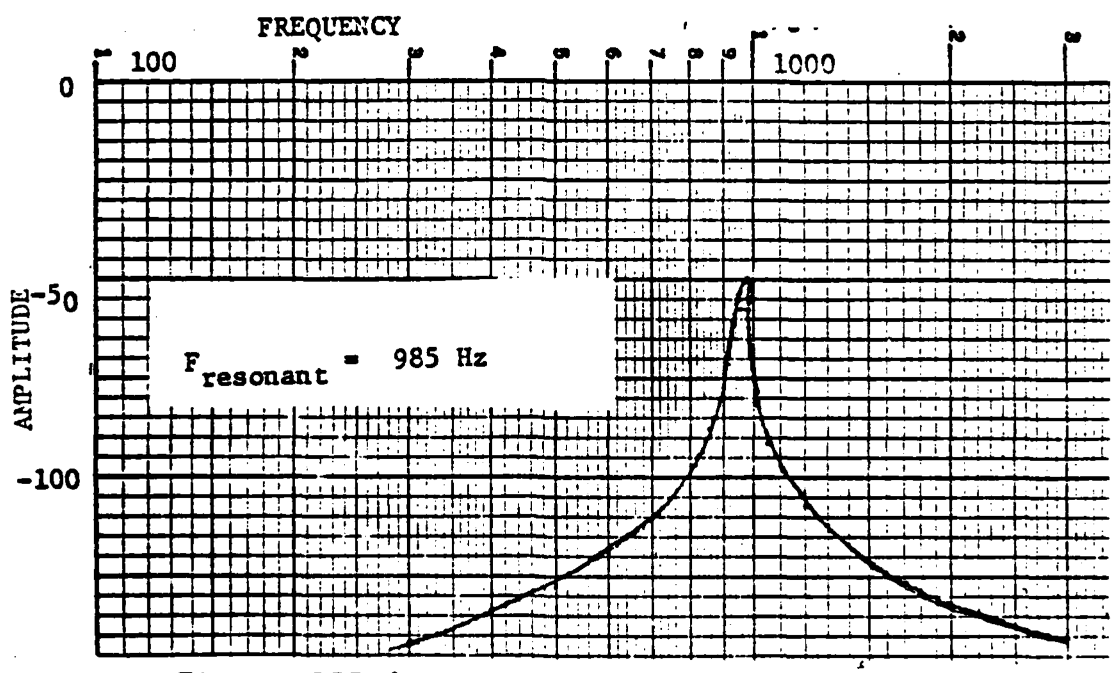

Figure III-6 Theoretical frequency response of analog resonant circuit

Figure III-7 shows input (upper trace), output (lower trace) waveforms at resonant frequency (1050 Hz). Figure III-8 and III-9 shows the same waveforms at 850 Hz and 1150 Hz input signal frequency respectively.

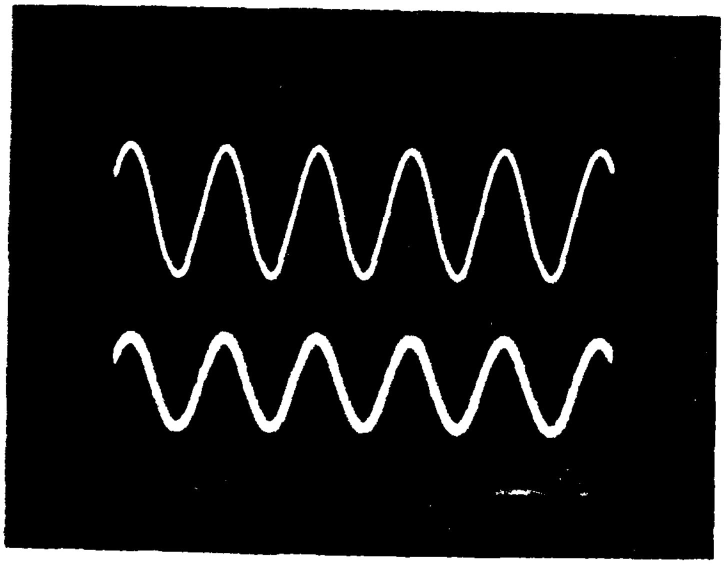

Figure III-7 Input (upper trace)- output (lower trace) waveforms of SC resonant circuit at resonant frequency.

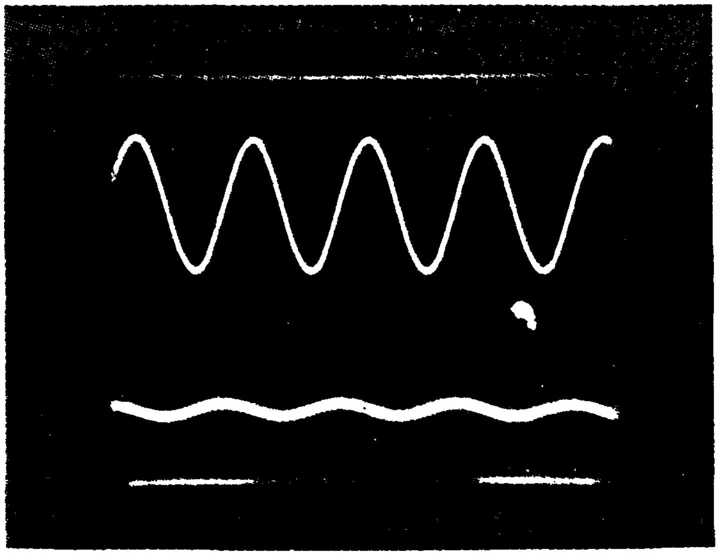

Figure III-8 Input (upper trace)- output (lower trace) waveforms of SC resonant circuit at 850 Hz input frequency.

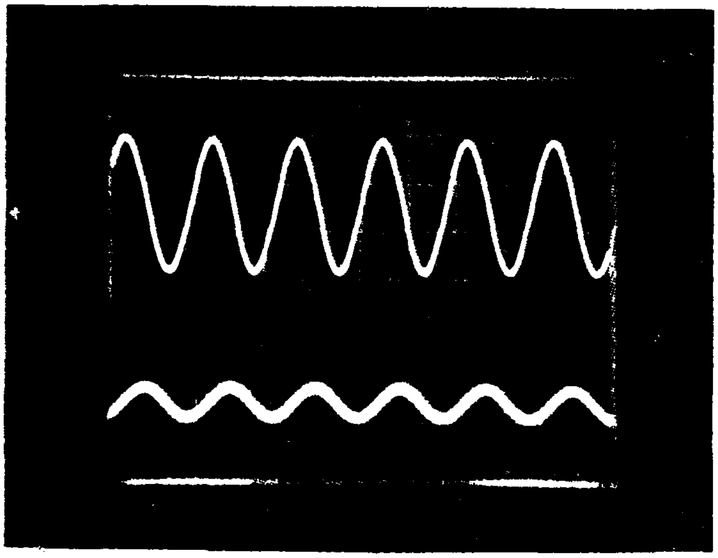

Figure III-9 Input-Output waveforms of SC circuit at 1150 Hz input signal

FLOATING INDUCTOR

In addition to grounded inductor, floating inductors can also be designed using SC circuits. The analysis given in the previous section is applicable for the floating inductor as well. The equivalent SC circuit is shown in Figure III-10.

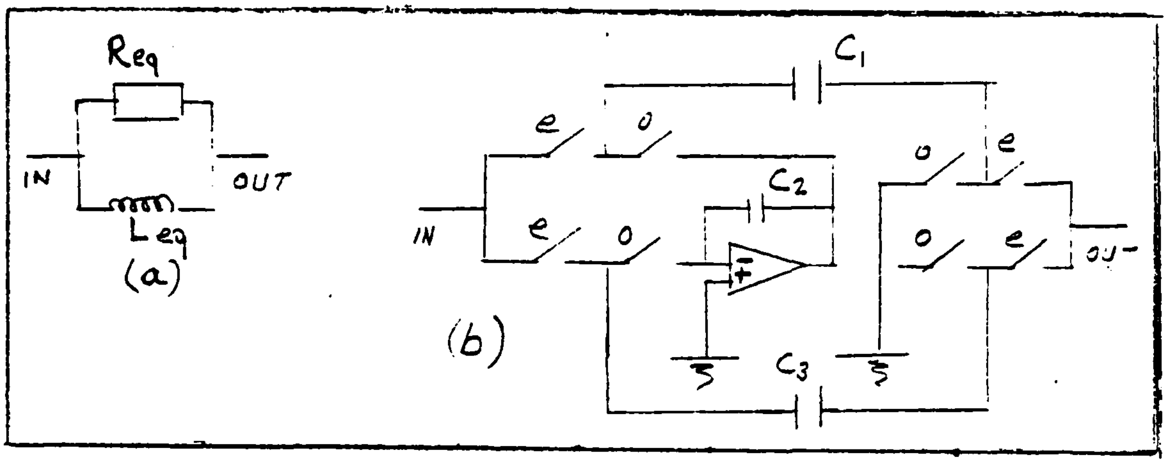

Figure III- 10 a) Floating inductor b) SC equivalent of (a). (Ref 13).

To demonstrate the SC floating inductor, the above circuit was incorporated in a low-pass filter design (Figure III-11). The equivalent analog circuit is given in Figure III-12. The SC circuit was designed using DG181 switches, SN72741 operational amplifier, and capacitors whose values are shown in Table III-2. $C_1 = C_3 = 2C_2$ was choosen so that R was open circuit or conductance is zero (see Eq. 3-20). The experiment was conducted for 16 Khz

Table III-2

<u>Capacitor values for SC circuit</u>

Capacitors	Capacitances
C_o	475 nF
C_1	822 pF
C_2	410 pF
C_3	822 pF
C	9.4 nF

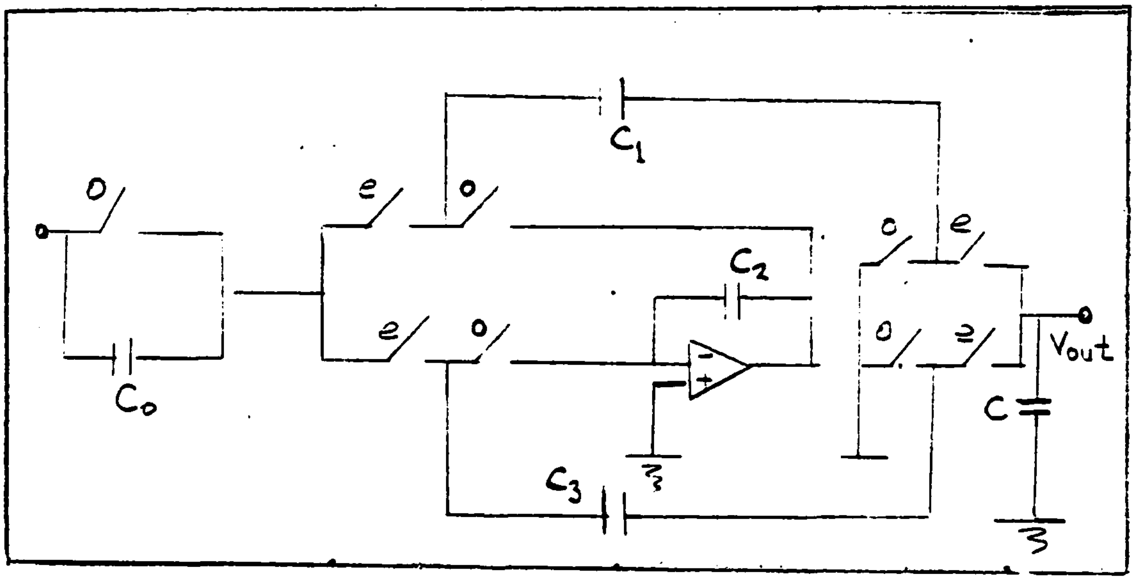

Figure III-11 SC low-pass filter

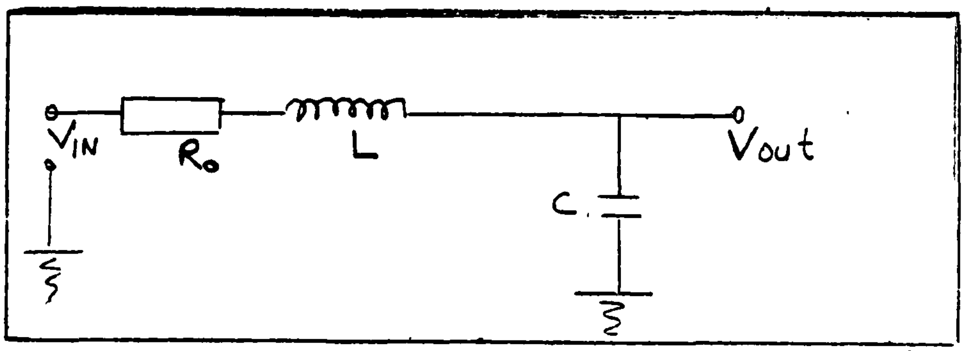

Figure III-12 Equivalent analog low-pass filter.

clock frequency. Based upon these values and Eqs. 3-17,18, the SC low-pass filter simulated a series resistor of 132 ohm, a series inductor of 2.37 H and a parallel capacitor of 9.47 nF. Figure III-14 shows the theoretical frequency responce of the analog circuit. Observed frequency responce of the SC circuit (Figure III-13) and Figure III-14 indicate an agreement between theory and experiment.

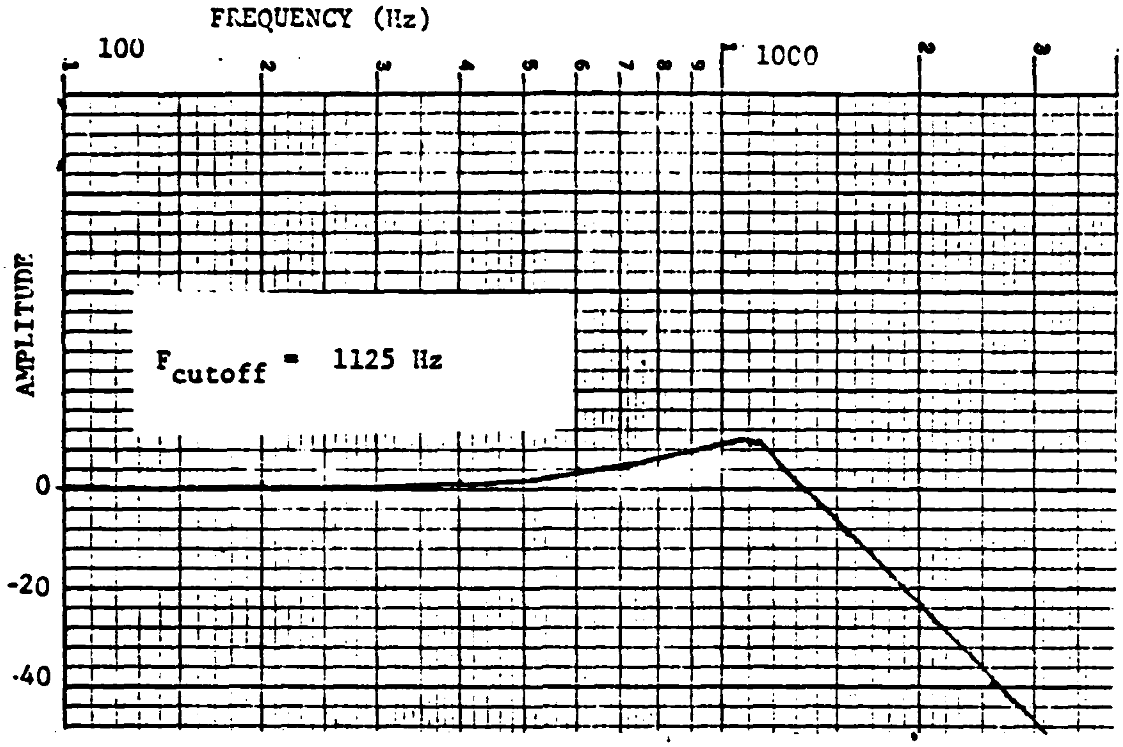

Figure III - 13 Frequency responce of SC Low-pass Filter

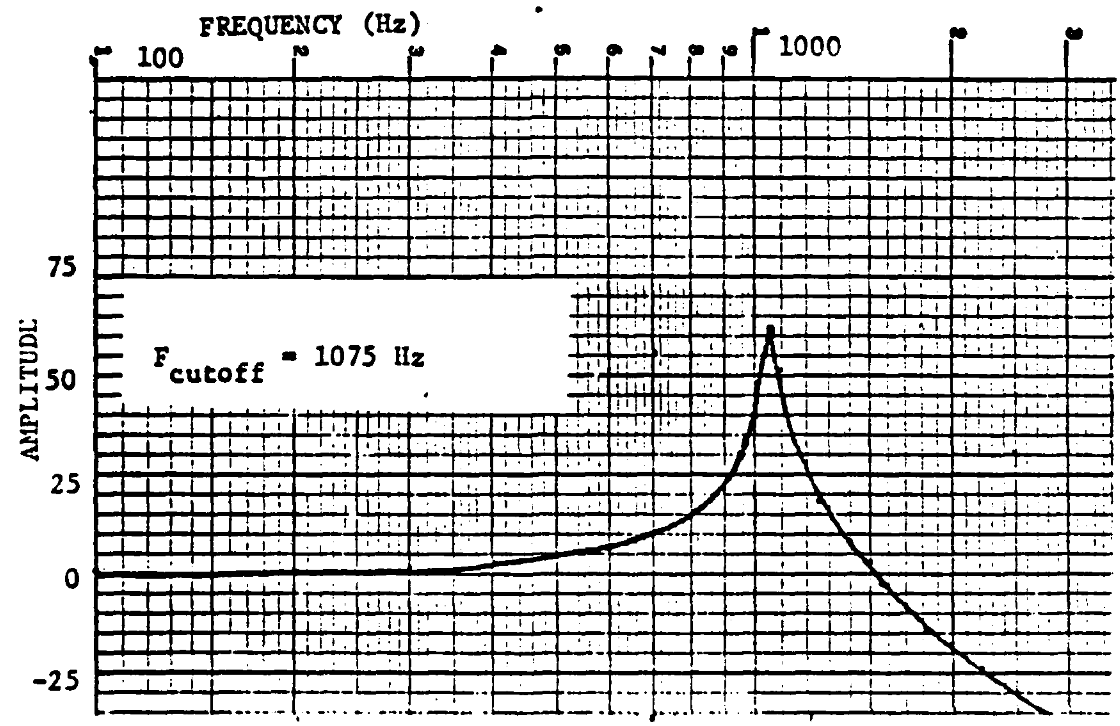

Figure III-14 Theoretical frequency responce of Analog Low-pass Filter

CHAPTER IV

SWITCHED-CAPACITOR SYNCHRONOUS DEMODULATOR

ANALYSIS AND DESIGN

One of the more important applications of the SC circuits is the realization of adaptive systems such as SC synchrous demodulators, channel equalizers, and tracking filters. There are many applications for synchronous demodulator, such as AM detection, FM detection, and phase detection. The SC synchronous demodulators are also useful to find real and imaginary components of a given system transfer function. A synchronous demodulator is easily realized using a SC low-pass filter which has only switched feedins. The paper by Martin and Sedra proposed a design for a SC demodulator using MOS transistors as switches (Ref 7).

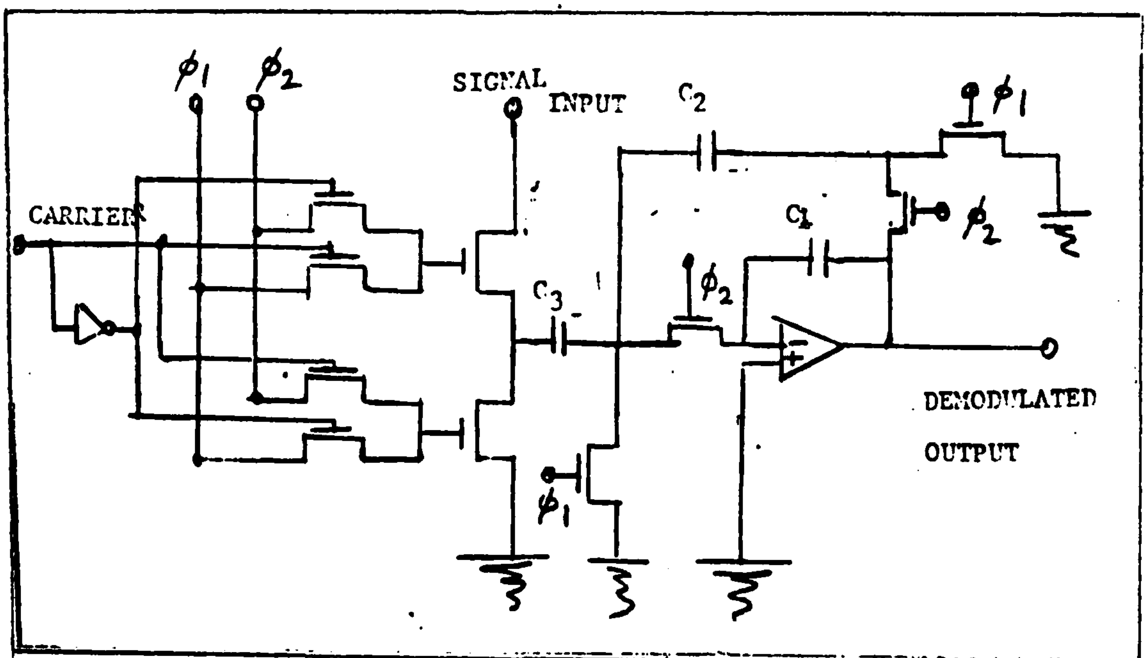

Figure IV-1 Proposed SC demodulator

The basic theory of operation of the proposed SC demodulator is to switch $Ø_1$ and $Ø_2$ at input of the SC low-pass filter. Alternating between $Ø_1$ and $Ø_2$ is equivalent to multiplying the input signal by +1 and -1 before applying it to the low-pass filter. The basic principles of the sampled data demodulation technique is presented in Appendix C.

The Figure IV-1 can be realized by using analog switches in place of MOS transistors. For proper operation of the proposed demodulator, the input signal must be sampled and then held constant for a full period (Ref 7). This eliminates any errors caused by the half period sampling time difference between $Ø_1$ and $Ø_2$. The circuit that accomplishes this is called a sample and hold circuit.

Sample and hold circuit

This circuit can be realized using analog switches, a flip-flop and a unity gain buffer which has high input impedance and a high slew rate As illustrated in Figure IV-2, when Q is high , the modulated input will be sampled, and C_2 will charge while C_1 charges or discharges through the op-amp input impedance. Since the op-amp has high input impedance, the rate of discharge will be very small. When Q goes low, the modulated input will be sampled and C_1 will charge or discharge while C_2 is connected to op-amp input. Since the clock applied to D flip-flop is either $ø_1$ or $Ø_2$, the operation of the circuit will be in sync with $\emptyset_1$ or $\emptyset_2$. The values of C_1 and C_2 will determine the time elapsed during charging of the capacitors. A typical value used for C_1 and C_2 is on the order of $1\,\mu F$.

Switching phases

Switching $\emptyset_1$ and $\emptyset_2$ at the input of low-pass SC filter can be accomplished using an analog switch (see Figure IV-3). When input is a leading edge-triggered carrier signal, $\emptyset_1$ is output from pins 2 and 5, while $\emptyset_2$ is output from pins 10 and 13. When input is a trailing edge-triggered carrier signal, $\emptyset_2$ is output from pins 2 and 5, while $\emptyset_1$ is output from pins 10 and 13. These outputs will be applied to the SC low-pass filter (Figure IV-4) to control the switching action at the input of the filter. As it was mentioned before , the carrier must be a square wave for the proper operation of the proposed SC demodulator.

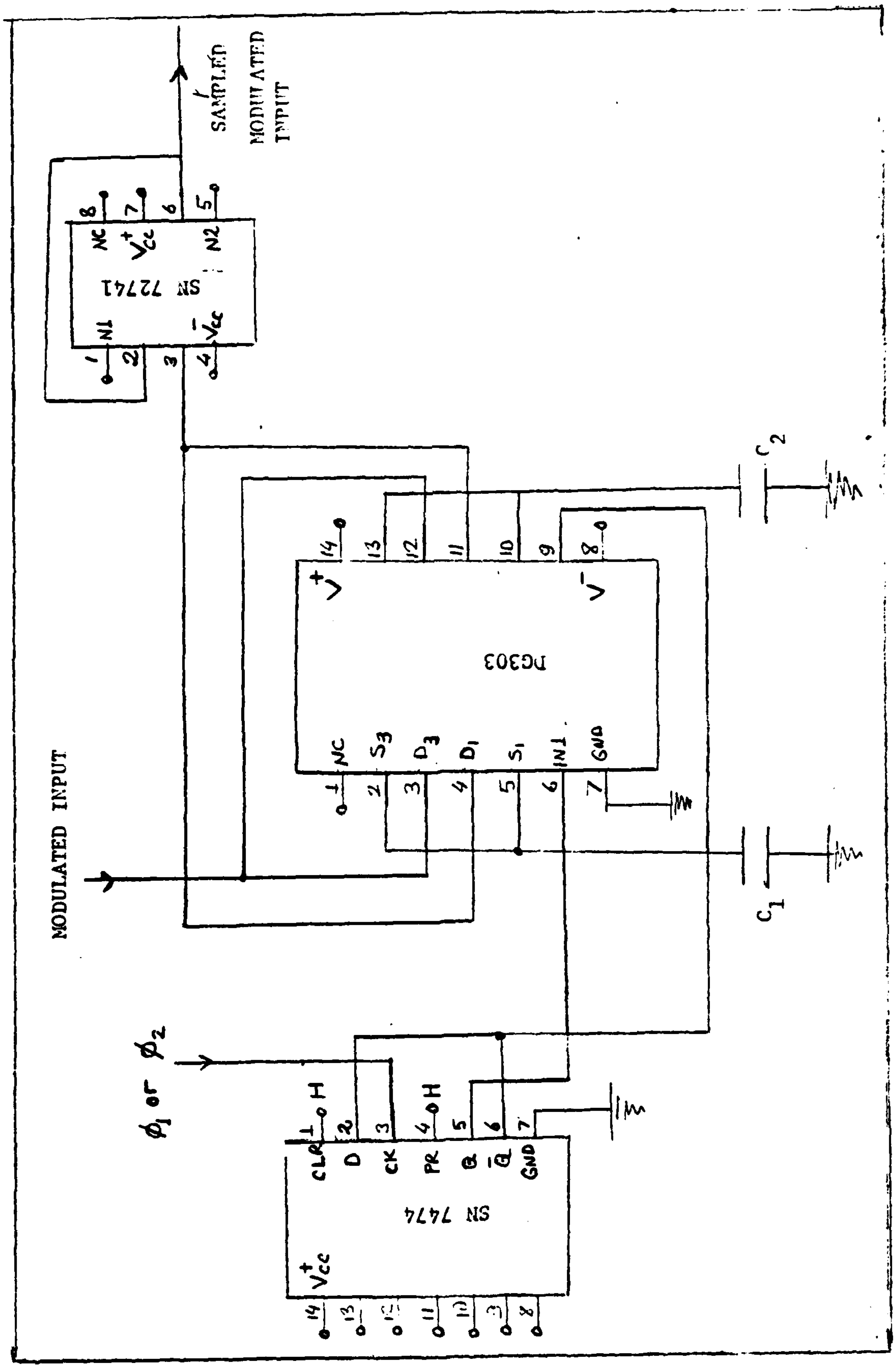

Figure IV - 2 Sample and Hold Circuit.

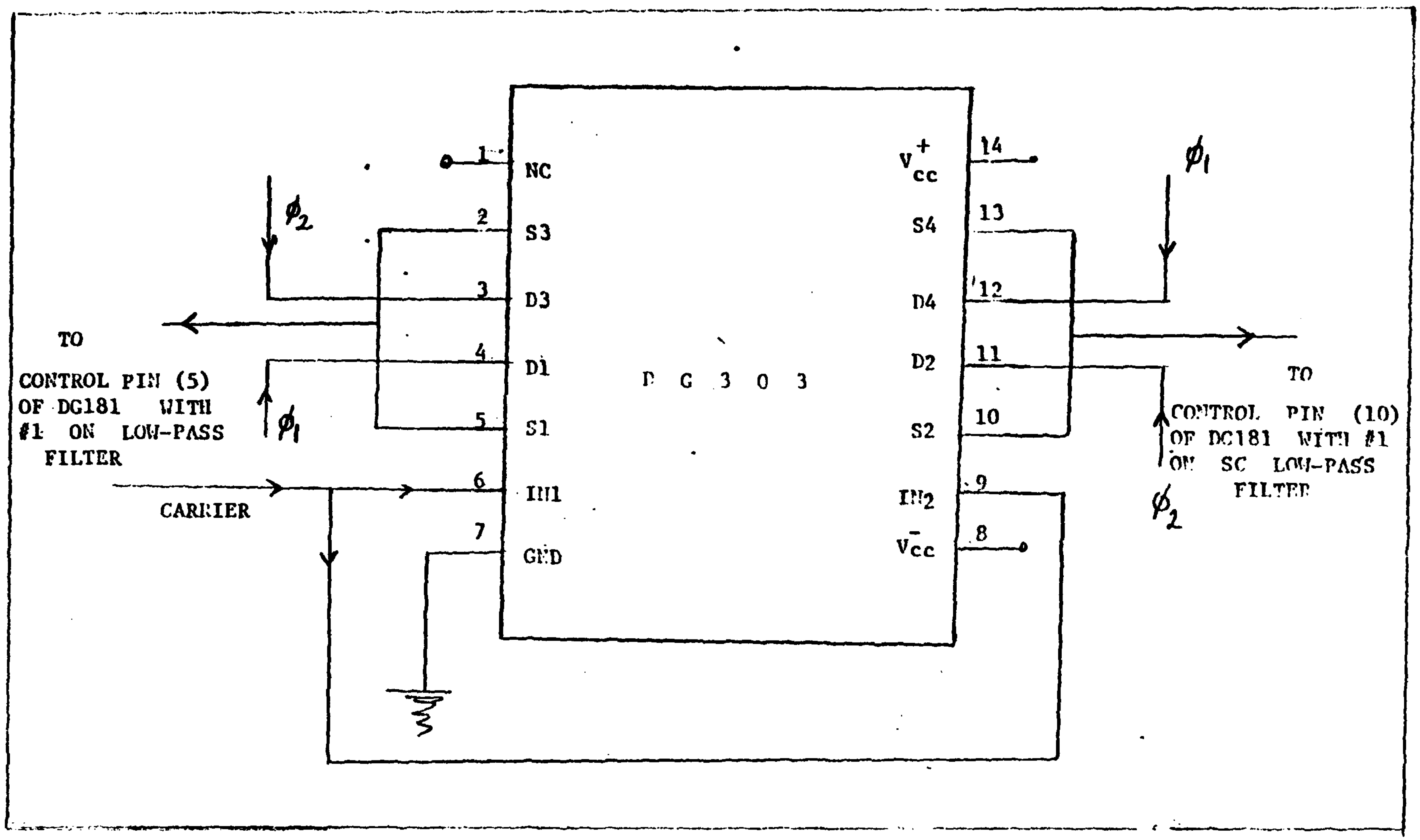

Figure IV - 3 Switching Circuit.

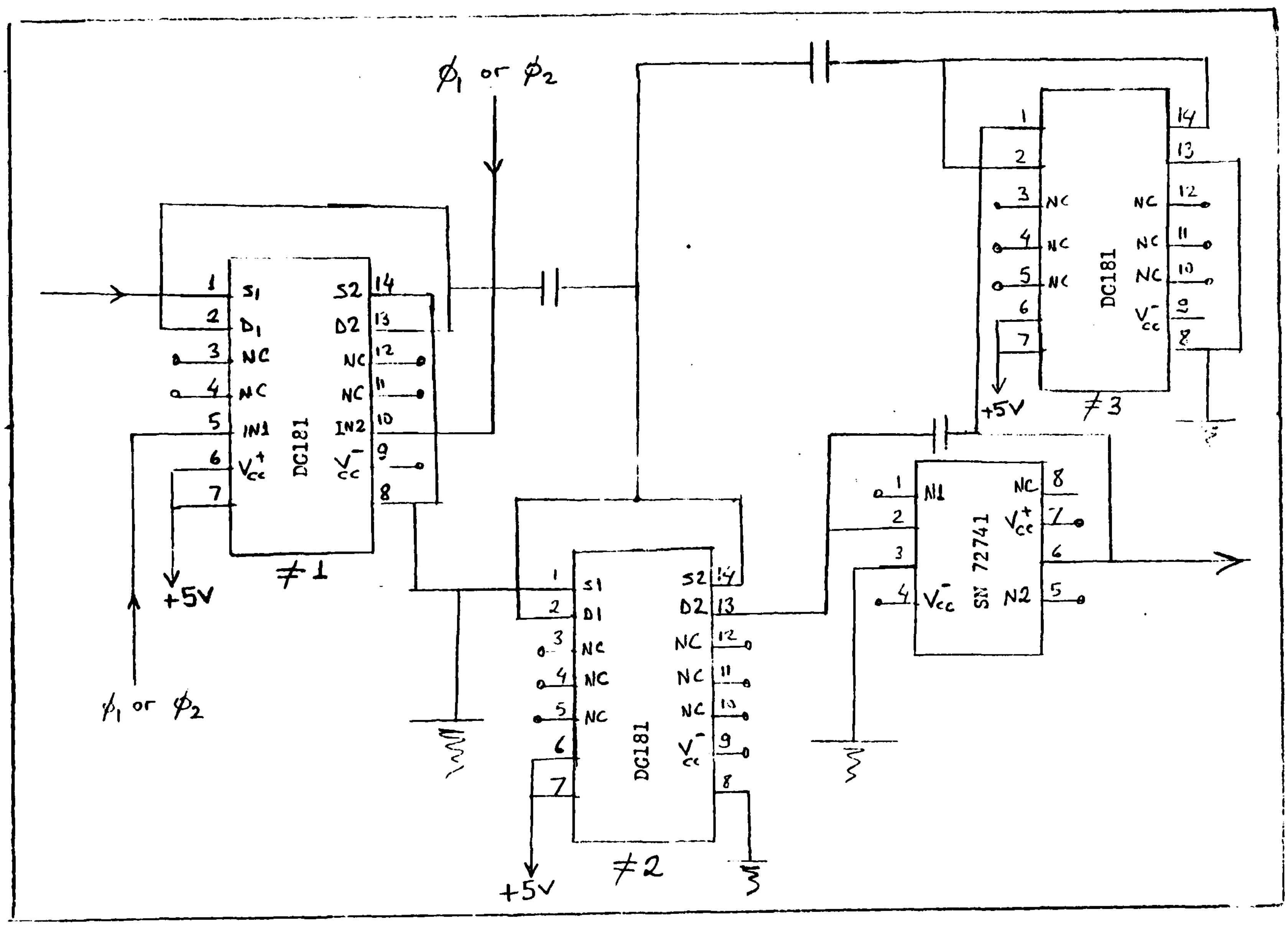

Figure IV - 4 SC Low-pass Filter.

FABRICATION AND TEST

A sample and hold circuit, switching circuit and SC low-pass filter were built using a 50 Khz clock frequency. The experiment was conducted for lower clock frequencies, but the output waveform was distorted. The sample and hold circuit was built using a SN7474 for the D flip-flop, a SN72741 for the op-amp and a DG303 for the analog switch. The DG303 is a single pole double throw analog switch. A detailed description of it is given in the Appendix D. The values used for capacitor C_1 was 1,023μF and for the capacitor C_2 was 0,969μF. The switching circuit was built using a DG303. The SC low-pass filter was built using a SN72741for the op-amp and a DG181 for each analog switch. The DG181 is a single pole single throw switch. The values 1000 pF, 100 pF, 0,01μF were used for C_1, C_2, and C_3 respectively. The modulated input signal was generated by using a WAVETEC 20 Mhz AM/FM/PM generator model 148.

For the modulated input signal, a 200 Hz sine wave modulated a high frequency sine wave carrier. Figure IV-6 shows the modulating signal (upper trace) and the carrier used for demodulation. The experiment was conducted for carrier frequencies of 100 Khz, 1 Mhz, 5 Mhz and 6 Mhz. A clear demodulated output was observed at 5 Mhz and 6 Mhz. The output was unrecognizably corrupted by noise at 100 Khz and 1 Mhz. Distortion occured when the carrier frequency for modulation differed from the carrier reference at the demodulator. The cutoff frequency of the SC low-pass filter was choosen as 225 Hz. That can be changed by changing the values of C_1, C_2, C_3.

The experiment was conducted for different modulation indices of input signal. It was observed that, for a higher modulation index less distortion occured. Figure IV-6 shows 100 percent modulated signal (upper trace) and demodulated signal (lower trace). Figure IV-7 shows 30 percent modulated signal (upper trace) and demodulated signal (bottom trace).

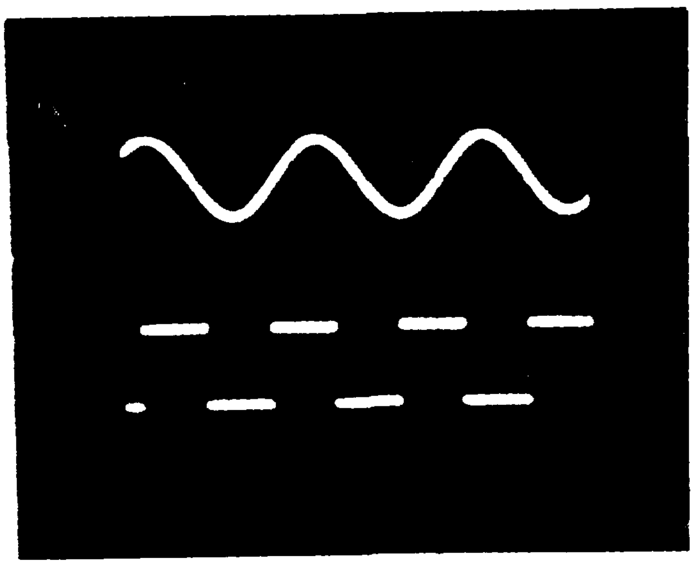

Figure IV-5 Modulating signal (upper trace) and SC demodulator carrier.

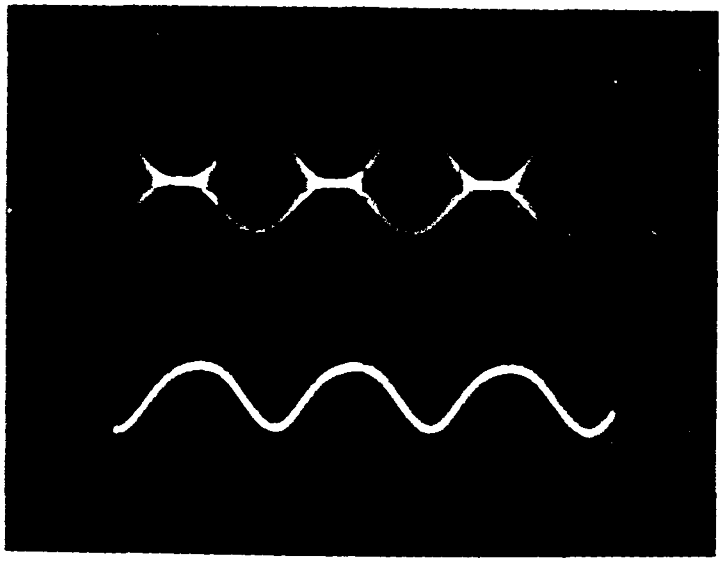

Figure IV-6. 100 percent modulated input signal (top trace) and demodulated signal

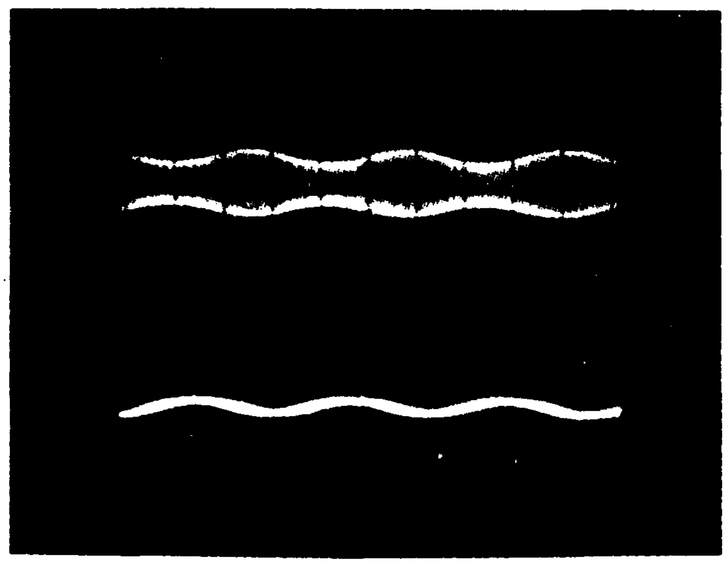

Figure IV-7 30 percent modulated input signal (top trace) and demodulated signal.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

In this study SC application of band elimination filter, simulation of inductors and realization of SC synchronous demodulator were experimentally investigated. For this purpose different technical papers claiming different characteristics about these circuits were examined. On the basis of the research performed, the following conclusions are made :

1. RC filter characteristics can be duplicated using switched-capacitors in place of resistors.
2. For proper operation of the SC circuits, the clock frequency must be much higher than the maximum signal frequency.
3. The SC filter bandwidth can be changed either by changing clock frequency or capacitor ratios.
4. Noise due to the amplifiers and the switches can be minimized by increasing clock frequency and capacitor sizes.
5. The stray capacitance between lower plate of the capacitor and ground can be minimized either by grounding the lower plate or by switching the both sides of the capacitor.

6. For a SC demodulator, the carrier frequency must be much higher than the modulating signal frequency.

7. SC resonant circuit which was built using SC circuits in place of resistors and inductor gave sharp peak at resonant frequency, as analog circuit.

RECOMMENDATIONS

Based on the results obtained in this study, the following recommendations are suggested :

1. For the clock circuit built , the overlaping time of phase one ($\emptyset_1$) and phase two ($\emptyset_2$) was 1/8 of the clock period. In order to improve the circuit performance, further study could be performed investigating the effect of varying this parameter.

2. Analog switches were used throughout the experiment. The experiment could be performed using MOS transistor switches for the same purpose to investigate circuit performance.

3. As op-amp, SN72741 was used throughout the experiment. For high frequency applications , op-amps which have better high frequency characteristics could be used.

4. The experiment in Chapter II was conducted for just band elimination filter. That shoud be expended for all kinds of filters (bandpass, lowpass, notch, etc...).

5. One of the important applications of the SC demodulator is to measure the quadrature components of the given system transfer function. This aspect of SC technique could be investigated.

6. Major application areas of the SC circuits are filtering, A/D or D/A conversion and realization of adaptive systems. For this experimental investigation, SC application of filters, an adaptive system and simulation of inductor were investigated. This experiment can be expended to SC application of A/D, D/A conversion technique, signal processing technique and realization of other adaptive systems such as channel equalizer phase lock loop, tracking filter.

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APPENDIX A

OPERATION OF SWITCHED-CAPACITORS

The basic principle of the switched-capacitor (see Figure A-1) resistor is to transfer a charge from point A to point B by charging the capacitor at point A and then discharging it through point B.

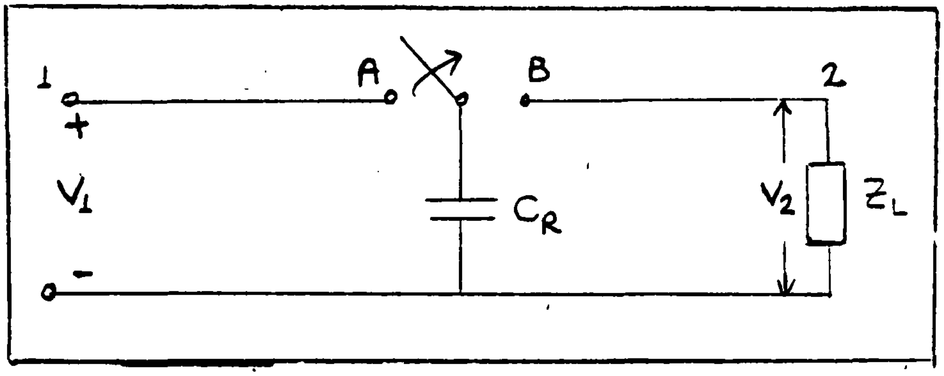


Figure A-1 Basic switched-capacitor circuit.

The analysis of the circuit (Ref 1:409) is performed by first examining its behaviour when the switch is in position A and then in position B.

Let us first assume that the input voltage v_1 is constant and the switch is initially in the position A. The capacitor C_R will thus be charged to the voltage v_1. This charging process is extremely fast relative to the switching cycle. For most practical purposes, it is assumed that the capacitor is charged instantaneously to the input voltage v_1. This is the case for an ideal switch. It is also assumed that the period of the clock which drives the switch is small enough so that the input signal (v_1) does not appear to change during one period of the clock. Thus, even if the input voltage v_1 is a function of time, the capacitor appears to instantaneously charge to v_1 as if we had an ideal switch connection.

If the switch is now changed to position B, the capacitor discharges at rate $\frac{dq}{dt}$ which is dependent upon the load impedance Z_L. Thus, V_2 is a time varying signal whose amplitude depends upon $Z_L \frac{dq}{dt}$.

The capacitor is, thus first charged to v_1 by the input signal, and then discharged to v_2 at the output end, in one period of the two phase clock. Moreover, this process is repeated in each period of the clock. There is thus a net charge transferred to the output side. The charge transferred by the capacitor in one clock period, to the terminal 2 will be

$$q = C_R(v_1 - v_2) \qquad (A - 1)$$

and this will be accomplished in time τ_c, the period of the clock. During this time interval, the current is simply

$$i(t) = \frac{\Delta q}{\Delta t} = \frac{C_R(v_1 - v_2)}{\tau_c} \qquad (A - 2)$$

Alternatively, the same result could be obtained if an appropriate resistor is placed between terminals 1 and 2 as in Figure A-2.

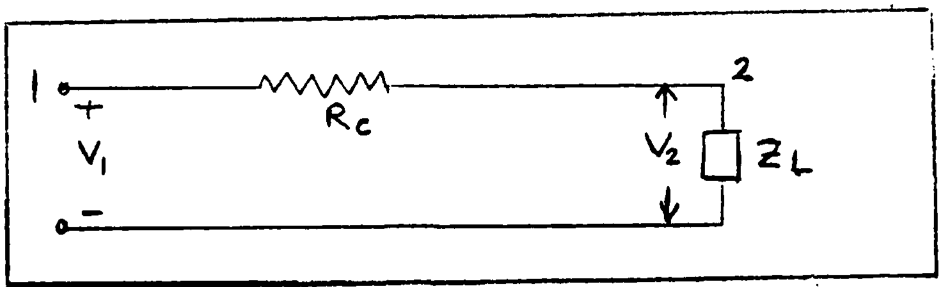


Figure A-2 Equivalent circuit of Figure A-1.

then

$$i(t) = \frac{1}{R_c}(v_1 - v_2) \qquad (A - 3)$$

By equating the Eqs. A-2 and A-3, the size of such an equivalent resistor which yields the same value of current, during this same time interval, is

$$R_c = \frac{v_1 - v_2}{L} = \frac{\tau_c}{C_R} = \frac{1}{f_c C_R} \qquad (A - 4)$$

where f_c is the clock frequency. Detailed circuit design of two phase non-overlaping clock is given in Appendix B.

For the approximation of Eq. A-2 to be valid, the switching frequency f_c be much larger than maximum frequency of $v_1(t)$ and $v_2(t)$ as in the case for voice processing filters. The switched capacitor may then be regarded as a direct replacement for the resistor.

APPENDIX B

TWO PHASE NON-OVERLAPPING CLOCK

The two phase non-overlapping clock which was used for all of the experiments was designed using a four-stage Johnson octal counter (MC 14022) so that multiple phases could be produced as necessary. Appendix D shows pin configuration and functional waveforms of the Johnson counter. The Johnson counter has eight decoded outputs. For the clock circuit, eight of them were used, to produce two phases with 1/8 of the period of overlapping time. Depending on the application, this overlapping time can be increased by letting the counter count until certain number and reset.

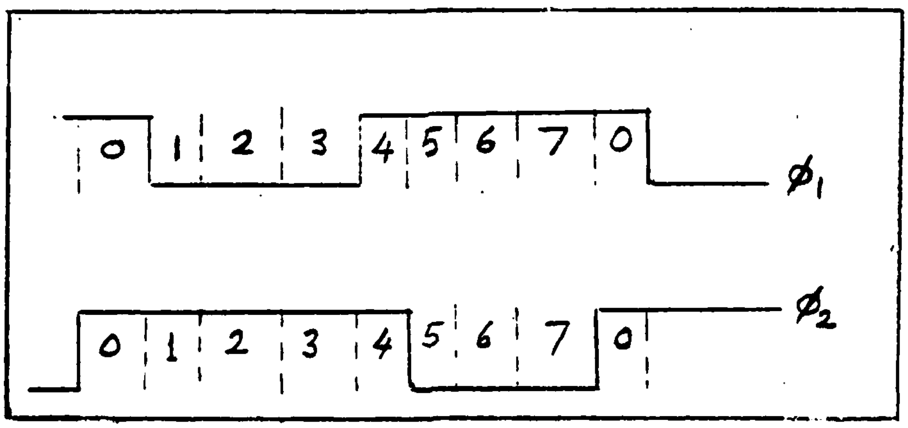


Figure B-1 Overlapping time of the phases

On the clock circuit (Figure B-2), the schmith invertor was used instead of normal invertor to get rid of transient spikes produced during the clock pulses.

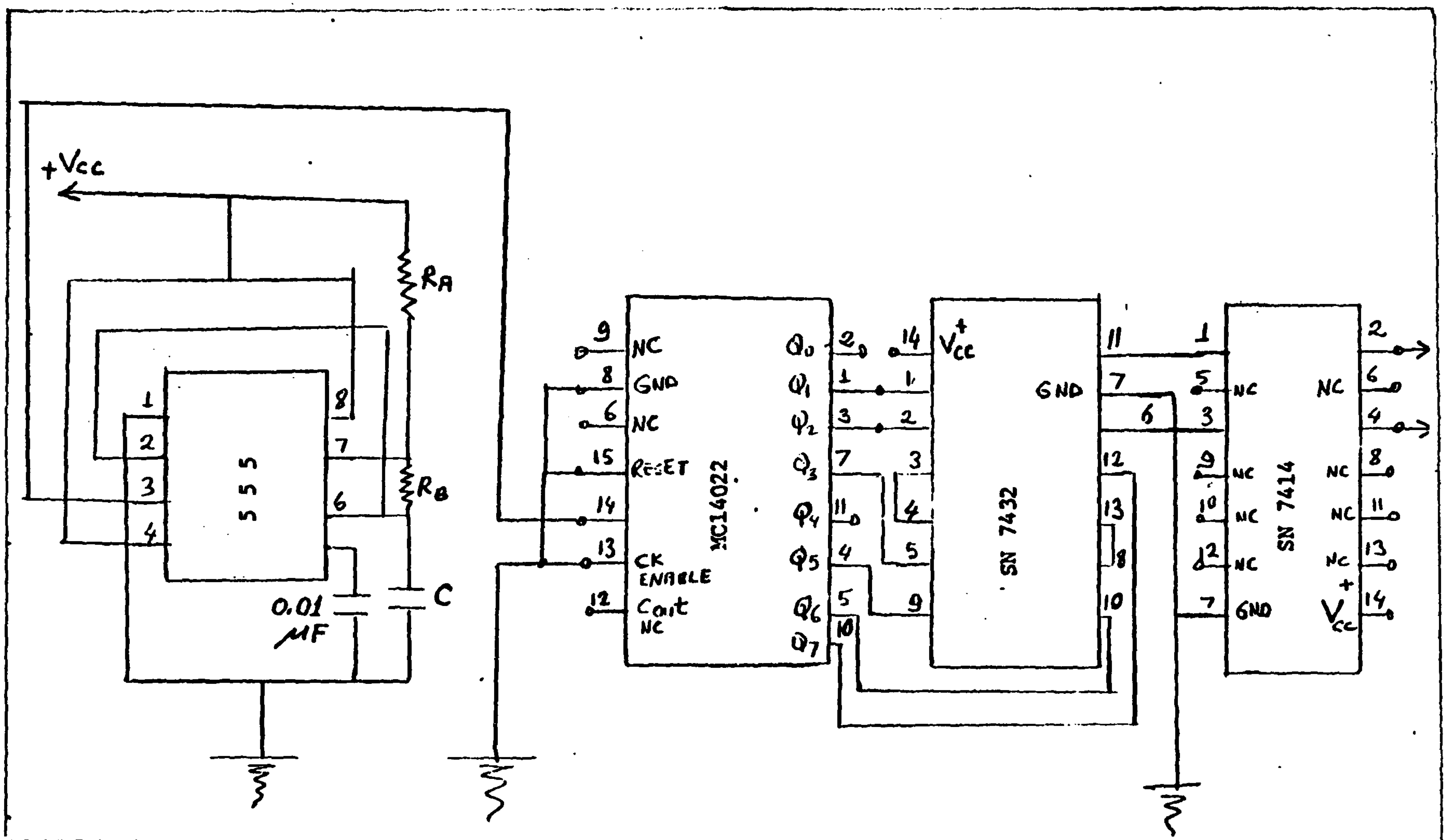


Figure B - 2 Two phase non-overlapping Clock Circuit.

How to change clock frequency

The clock frequency can be changed by changing the frequency of the output of the MC1555 timer. This is accomplished by changing the values of R_B, R_A, or C on the circuit of the timer. These component values are related to the timer period by the relatioship :

$$T = 0.693(R_A + 2R_B)C \qquad (B - 1)$$

For example : if f_c = 10 Khz clock frequency is needed and if eight counts are used, then the frequency of the output of the MC1555 timer is going to be 8x10 = 80 Khz or

$$T = \frac{1}{f} = \frac{1}{80 \times 10^3} = 12.5\,\mu\text{ sec} \qquad (B - 2)$$

using

$$R_A = R_B = 25 \text{ k-ohms} \qquad (B - 3)$$

then the capacitor value needed is 240 pF.

Figure B-3 shows typical waveforms of phase one ($\emptyset_1$) and phase two ($\emptyset_2$). The signal frequency is 3333,3 Hz.

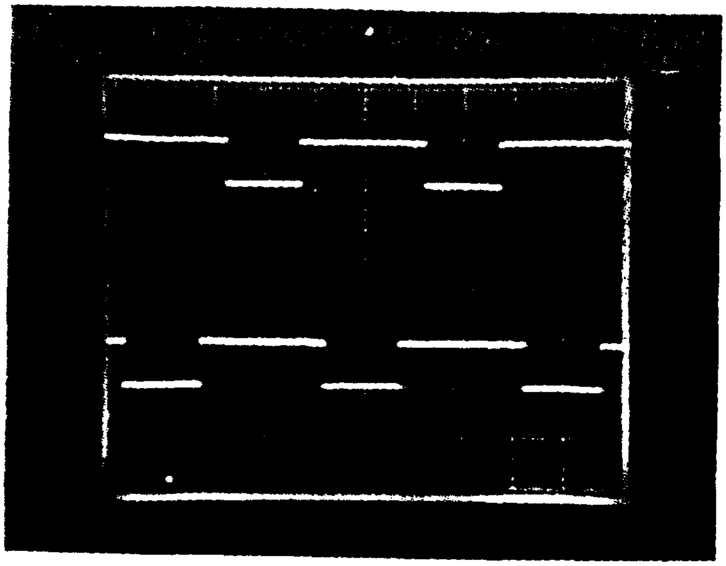


Figure B-3. Clock phases.

Horizontal: 0.2 ms/div

Vertical: 5 V/div.

APPENDIX C

SAMPLED DATA DEMODULATION

If samples completely specify a signal, it should be possible to recover the signal from the samples. This is the demodulation process required for sampled data or pulse modulation systems. One of the main characteristics of the demodulation is to use the same carrier frequency for the modulation and demodulation. A simpler form of demodulation is to pass the sampled signal through a low-pass filter of bandwidth f (maximum signal frequency) hertz (Ref 14:99). This is shown in Figure C-1.

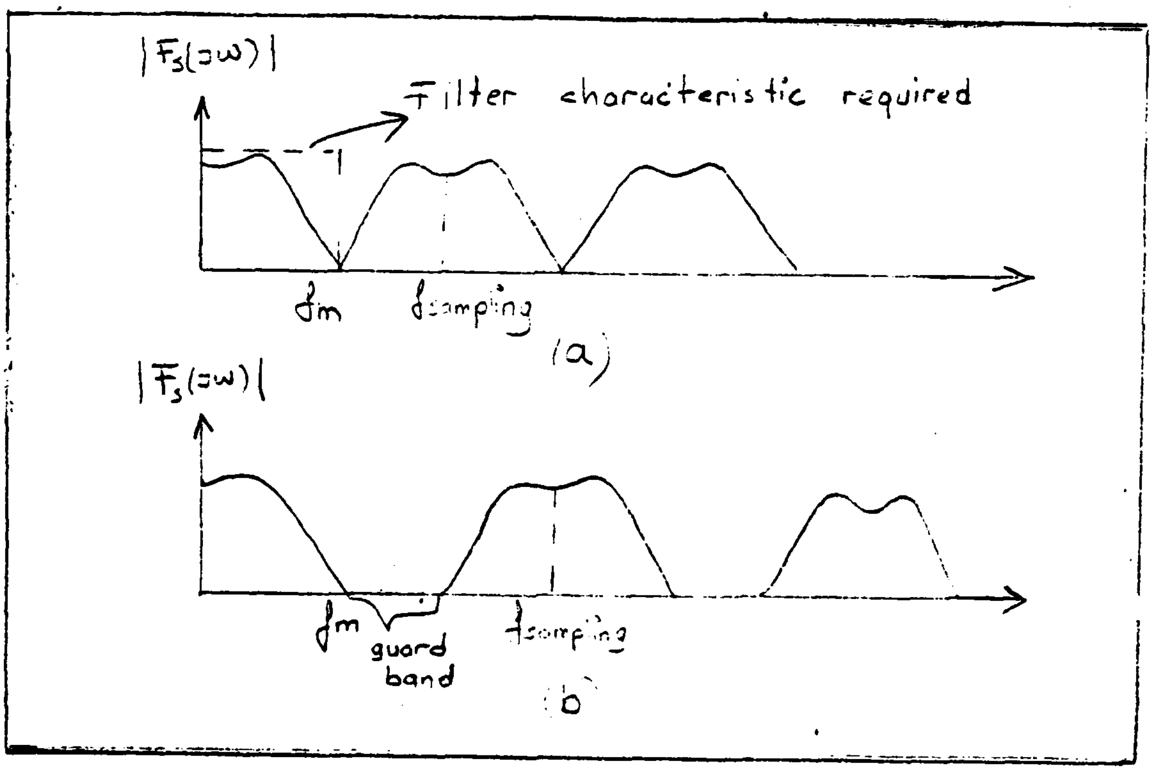


Figure C-1. Sampled data demodulation using low-pass filter. (a)$f_{sampling} = 2f_m$ (b)$f_{sampling} > 2f_m$

If we sample at exactly the Nyquist rate ($f_{sampling}$ - $2f_m$) the filter required must have ideal cutoff characteristics, as shown in Figure C-1a (Ref 14:99). This requires an ideal filter- an impossibility in practice. A practical low-pass filter with sharp cutoff characteristics could of course be used, with resulting complexity in filter design and some residual distortion. This situation can be relieved somewhat by sampling at higher rate, as shown in Figure C-1b. A guard band is thus made available and the filter requirements are less severe: the filter cutoff between f and $f_{sampling} - f_m$, and the attenuation at $f_{sampling} - f_m$ being some prescribed quantity measured with respect to the passband.

APPENDIX D

INTEGRATED CIRCUIT DATA SHEETS

This section contains data sheets for the principle integrated circuits which were used throughout the experiment. The data sheets contain electrical characteristics and pin configurations for each chip. Included in this section are data sheets for each of the following integrated circuit chips :

1.	MC14022	Johnson Octal Counter	(Ref 15:(7-71;7-75))
2.	555	Timer	(Ref 16: 1-4)
3.	DG181	Analog Switch	(Ref 17:(3-42;3-44))
4.	DG303	Analog Switch	(Ref 17:(3-79;3-80))
5.	SN72741	Operational Amplifier	(Ref 18:(3-34;3-35))

MC14022AL
MC14022CL
MC14022CP

COUNTER

OCTAL COUNTER/DRIVER

The MC14022 is a four-stage Johnson octal counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting when used with MC14001 NOR Gate
- Pin-for-Pin Replacement for CD4022A

McMOS

(LOW POWER COMPLEMENTARY MOS)

OCTAL COUNTER/DIVIDER

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14022AL MC14022CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14022AL – MC14022CL/CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

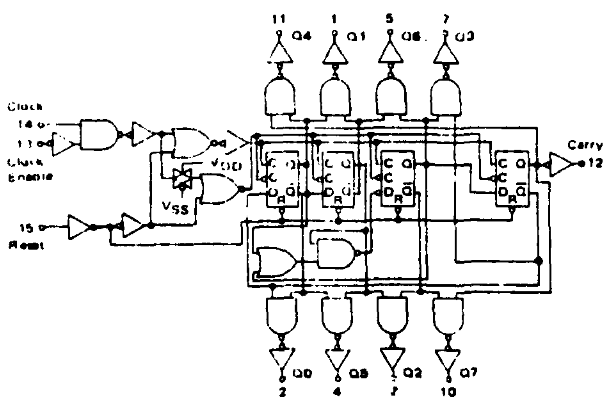
FUNCTIONAL TRUTH TABLE

(Positive Logic)

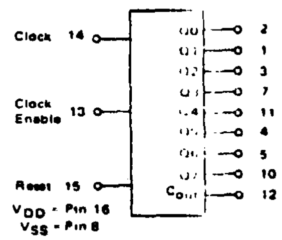
CLOCK	CLOCK ENABLE	RESET	OUTPUT = n
0	X	0	n
X	1	0	n
↑	0	0	n+1
↓	X	0	n
1	↓	0	n+1
X	↑	0	n
X	X	1	Q0

X = Don't Care   If n < 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



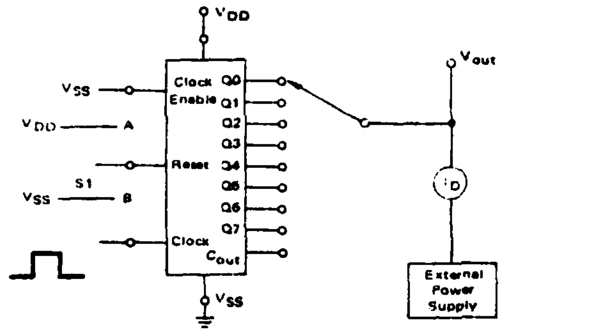
V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Follow ing PAGES

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	Output Sink Drive	Output Source Drive
Outputs	(S1 to A)	Clock to desired output (S1 to B)
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

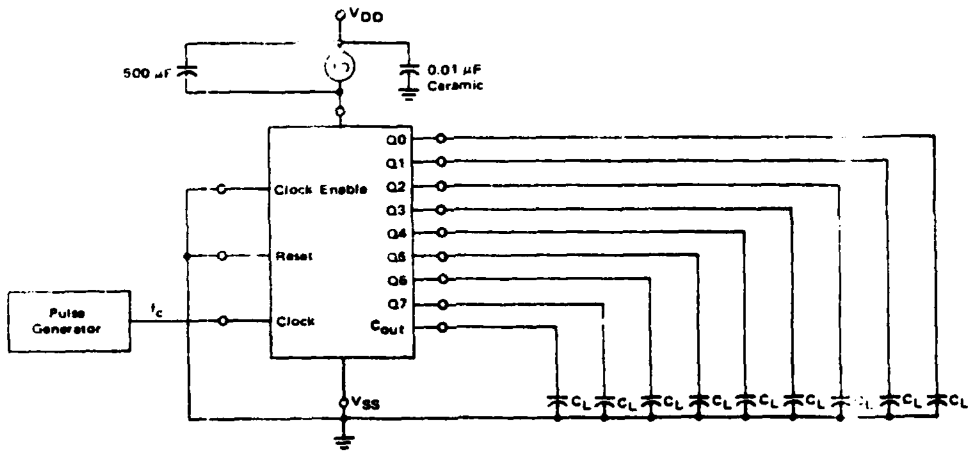
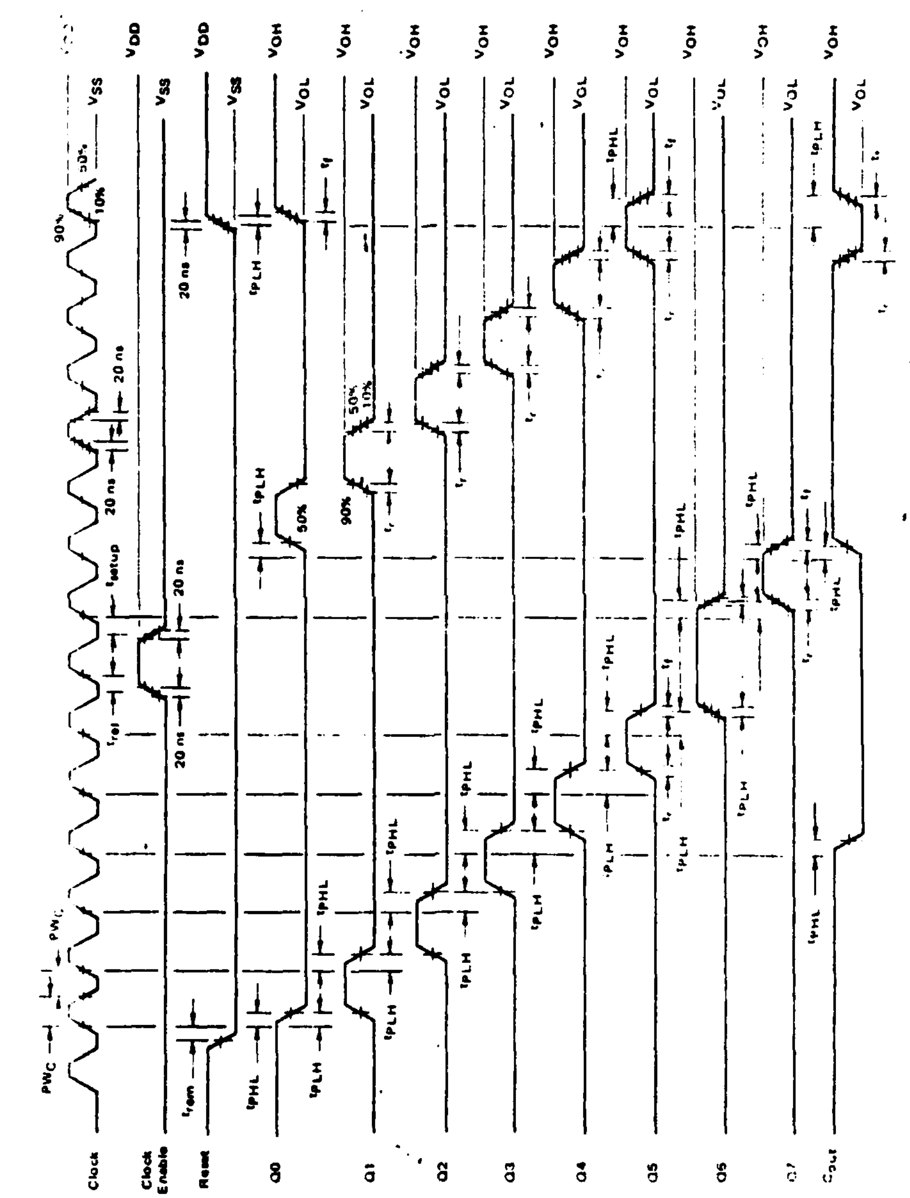


FIGURE 3 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



signetics

TIMER 555

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

FEATURES

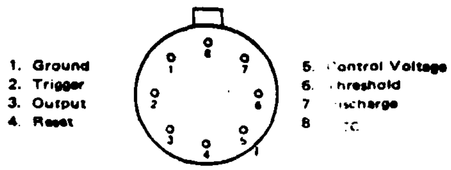
- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.05% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

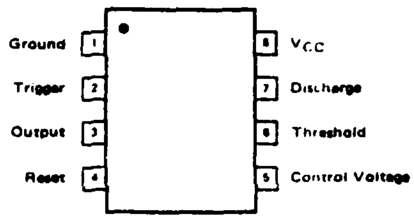
PIN CONFIGURATIONS (Top View)

T PACKAGE



ORDER PART NOS. SE555T/NE555T

V PACKAGE

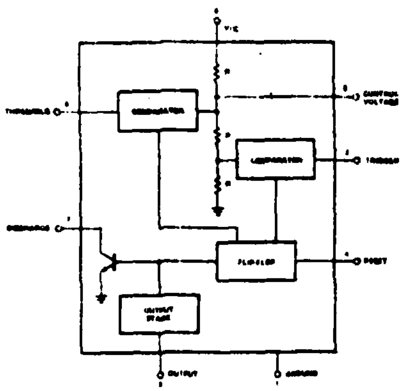


ORDER PART NOS. SE555V/NE555V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

BLOCK DIAGRAM



1

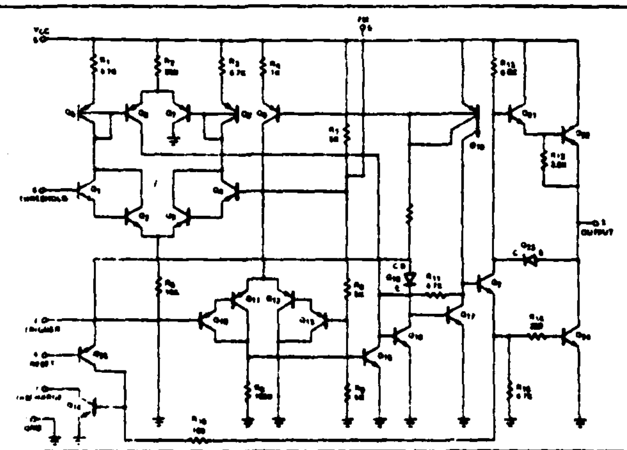
ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified

PARAMETER	TEST CONDITIONS	SE 555 MIN	SE 555 TYP	SE 555 MAX	NE 555 MIN	NE 555 TYP	NE 555 MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
	Low State, Note 1							
Timing Error	R_A, R_B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1 µF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		µA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	µA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					.25	.35	
Output Voltage Drop (high)								
	I_{SOURCE} = 200mA		12.5			12.5		
	V_{CC} = 15V							
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec

NOTES

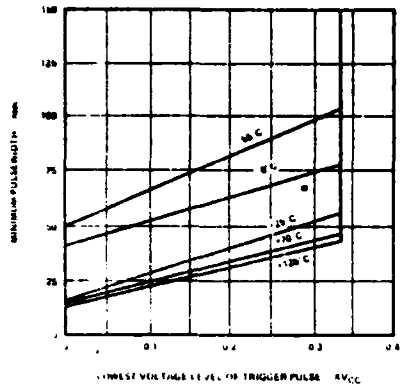
1. Supply Current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. This will determine the maximum value of R_A + R_B. For 15V operation, the max total R = 20 megohm.

EQUIVALENT CIRCUIT (Shown for One Side Only)

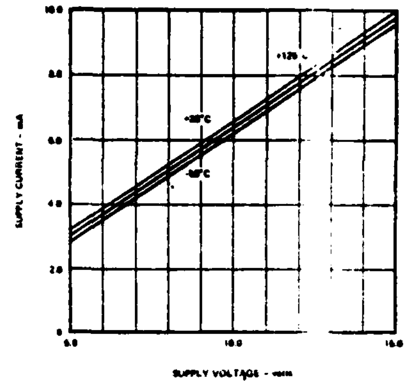


TYPICAL CHARACTERISTICS

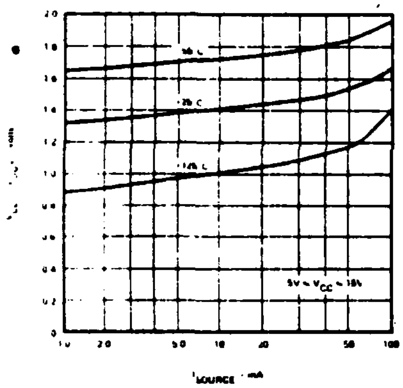
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



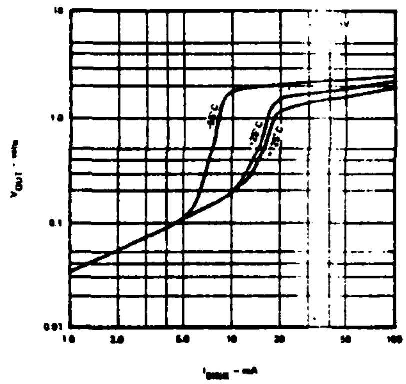
SUPPLY CURRENT vs SUPPLY VOLTAGE



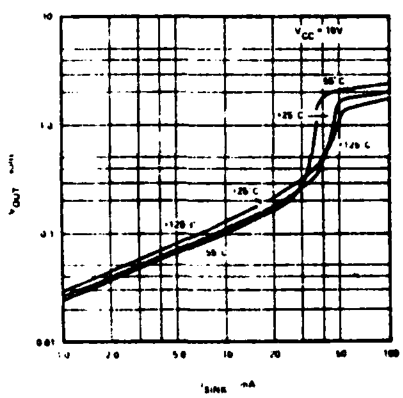
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



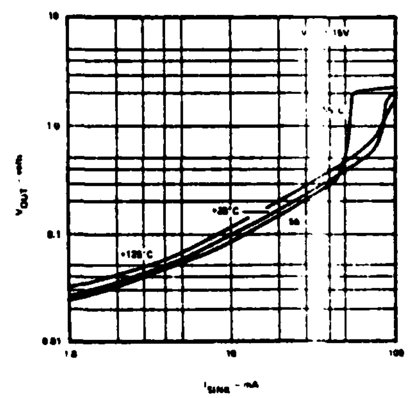
HIGH OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT



LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



High-Speed Driver with JFET Switches *designed for...*

Siliconix

- **Fast Acquisition Speed in Sample and Hold Circuits**
- **Low Leakage Switching Applications i.e. Sample and Hold Circuits**
- **High Frequency Signal Switching such as Video Signals**
- **Low Distortion Switching, Audio Signals**
- **Low Level Switching in Low Impedance Circuits**
- **Fast, Low Resistance D/A Ladders**

BENEFITS

- **Eliminates Large Signal Error**
  < 2 nA Leakage from Signal Channel in Both ON and OFF States
- **Increased Current Handling Capabilities**
  200 mA Maximum Switching Current
- **Higher Bandwidth Switching Capabilities**
  Cross Talk and OFF Isolation > 55 dB at 1 MHz (75 Ω Load)
- **Easily Interfaced**
  TTL, DTL, RTL Direct Drive Compatibility
- **Less Signal Distortion than CMOS or PMOS Switches**
  Constant ON Resistance
- **Low Voltage Drop Across Switch in the ON State**
  $r_{ds(on)} \leq 10\ \Omega$

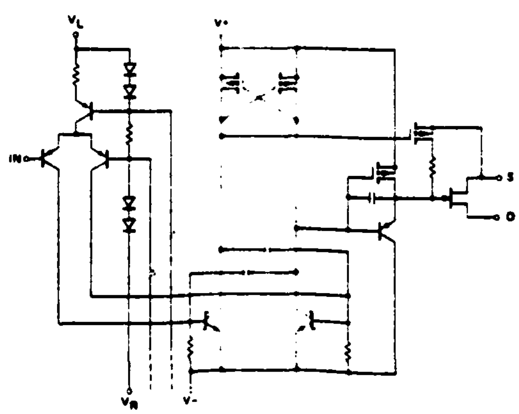
DESCRIPTION

The DG180 series contains two to four N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.0 V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 20 V peak-to-peak. Switch-OFF input-output feed-through is > 60 dB at 10 MHz, because of the low output impedance of the FET-gate driving circuit.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON} (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75

SCHEMATIC DIAGRAM (Typical Channel)



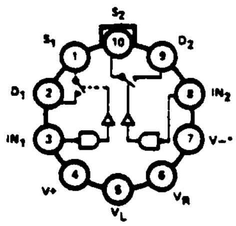
PIN CONFIGURATIONS

DUAL SPST

LOGIC	SWITCH
0	ON
1	OFF

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

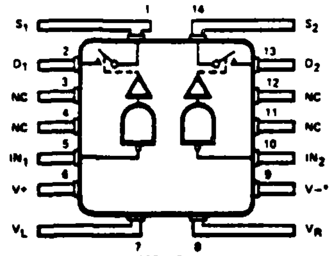
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG180AA OR DG180BA
DG181AA OR DG181BA
DG182AA OR DG182BA
SEE PACKAGE 2
*Common to Substrate and Case

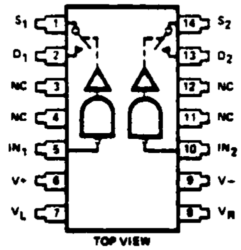
Flat Package



TOP VIEW

ORDER NUMBER:
DG181AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



TOP VIEW

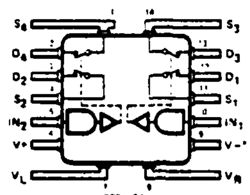
ORDER NUMBERS:
DG180AP OR DG180BP
DG181AP OR DG181BP
DG182AP OR DG182BP
SEE PACKAGE 11

DUAL DPST

LOGIC	SWITCH
0	OFF
1	ON

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

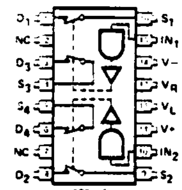
Flat Package



TOP VIEW

ORDER NUMBERS:
DG184AL OR DG185AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



TOP VIEW

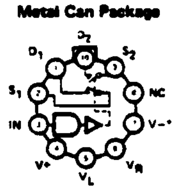
ORDER NUMBERS:
DG183AP OR DG183BP
DG184AP OR DG184BP
DG185AP OR DG185BP
SEE PACKAGE 12

SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

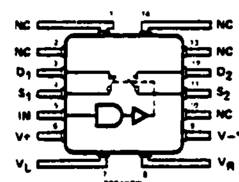
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG186AA OR DG186BA
DG187AA OR DG187BA
DG188AA OR DG188BA
SEE PACKAGE 2
*Common to Substrate and Case

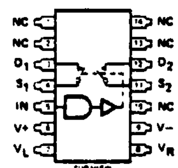
Flat Package



TOP VIEW

ORDER NUMBERS:
DG187AL OR DG188AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



TOP VIEW

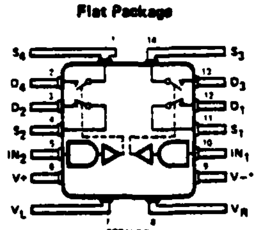
ORDER NUMBERS:
DG186AP OR DG186BP
DG187AP OR DG187BP
DG188AP OR DG188BP
SEE PACKAGE 11

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

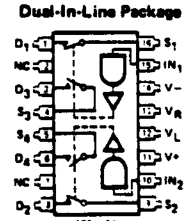
Flat Package



TOP VIEW

ORDER NUMBERS:
DG190AL OR DG191AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG189AP OR DG189BP
DG190AP OR DG190BP
DG191AP OR DG191BP
SEE PACKAGE 12

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	33 V
V_D to V−	33 V
V_D to V_S	±22 V
V_L to V−	36 V
V_L to V_{IN}	8 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V−	27 V
V_R to V_{IN}	2 V
Current (Any Terminal except S or D)	30 mA

Currents (S or D) 30 Ω, 75 Ω	30 mA
10 Ω Only	200 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Metal Can**	450 mW
14 Pin DIP***	825 mW
16 Pin DIP****	900 mW
Flat Pack*****	900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.
*****Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

Type		No.	Characteristic		MAX LIMITS A SUFFIX −55°C	25°C	125°C	B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_L = 5 V, V_R = 0	
10 Ω DG180, DG183, DG186, DG189	SWITCH	1	$r_{DS(on)}$	Drain Source ON Resistance	10	10	20	15	15	25	Ω	V_D = −7.5 V	I_S = −10 mA, V_{IN} = 0.8 V or 2.0 V, Note 1
		2	$I_{S(off)}$	Source OFF Leakage Current		10	1000		15	300	nA	V_S = 10 V, V_D = −10 V, V+ = 10 V, V− = −20 V	V_{IN} = 2.0 V or 0.8 V, Note 2
		3				10	1000		15	300		V_S = 7.5 V, V_D = −7.5 V	
		4	$I_{D(off)}$	Drain OFF Leakage Current		10	1000		15	300		V_D = 10 V, V_S = −10 V, V+ = 10 V, V− = −20 V	
		5				10	1000		15	300		V_D = 7.5 V, V_S = −7.5 V	
		6	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−200		−10	−200		V_D = V_S = −7.5 V	
		7	I_{DSS}	Saturation Drain Current	300 Typical*						mA	2 msec Pulse Duration	
	INPUT	8	I_{INL}	Input Current Input Voltage Low	−250	−250	−250	−250	−250	−250	µA	V_{IN} = 0	
		9	I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
	DYNAMIC	10	t_{on}	Turn-ON Time		300			350		ns	See Switching Time Test Circuit	
		11	t_{off}	Turn-OFF Time		250			300				
		12	$C_{S(off)}$	Source OFF Capacitance	21 Typical*						pF	V_S = −5 V, I_D = 0	f = 1 MHz
		13	$C_{D(off)}$	Drain OFF Capacitance	17 Typical*							V_D = 5 V, I_S = 0	
		14	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	17 Typical*							V_D = V_S = 0	
		15		OFF Isolation	Typical > 55 dB at 1 MHz*							R_L = 75 Ω	
30 Ω DG181, DG184, DG187, DG190	SWITCH	1	$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60	50	50	75	Ω	V_D = −7.5 V	I_S = −10 mA, V_{IN} = 0.8 V or 2.0 V, Note 1
		2	$I_{S(off)}$	Source OFF Leakage Current		1	100		5	100	nA	V_S = 10 V, V_D = −10 V, V+ = 10 V, V− = −20 V	V_{IN} = 2.0 V or 0.8 V, Note 2
		3				1	100		5	100		V_S = 7.5 V, V_D = −7.5 V	
		4	$I_{D(off)}$	Drain OFF Leakage Current		1	100		5	100		V_D = 10 V, V_S = −10 V, V+ = 10 V, V− = −20 V	
		5				1	100		5	100		V_D = 7.5 V, V_S = −7.5 V	
		6	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−200		−10	−200		V_D = V_S = −7.5 V	
	INPUT	7	I_{INL}	Input Current, Input Voltage Low	−250	−250	−250	−250	−250	−250	µA	V_{IN} = 0	
		8	I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
	DYNAMIC	9	t_{on}	Turn-ON Time		150			180		ns	See Switching Time Test Circuit	
		10	t_{off}	Turn-OFF Time		130			150				
		11	$C_{S(off)}$	Source OFF Capacitance	9 Typical*						pF	V_S = −5 V, I_D = 0	f = 1 MHz
		12	$C_{D(off)}$	Drain OFF Capacitance	6 Typical*							V_D = −5 V, I_S = 0	
		13	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14 Typical*							V_D = V_S = 0	
		14		Off Isolation	Typical > 50 dB at 10 MHz							R_L = 75 Ω	
75 Ω DG182, DG185, DG188, DG191	SWITCH	1	$r_{DS(on)}$	Drain-Source ON Resistance	75	75	150	100	100	150		V_D = −10 V	I_S = −10 mA, V_{IN} = 0.8 V or 2.0 V, Note 1
		2	$I_{S(off)}$	Source OFF Leakage Current		1	100		5	100	nA	V_S = 10 V, V_D = −10 V, V+ = 10 V, V− = −20 V	V_{IN} = 2.0 V or 0.8 V, Note 2
		3				1	100		5	100		V_S = 10 V, V_D = −10 V	
		4	$I_{D(off)}$	Drain OFF Leakage Current		1	100		5	100		V_D = 10 V, V_S = −10 V, V+ = 10 V, V− = −20 V	
		5				1	100		5	100		V_D = 10 V, V_S = −10 V	
		6	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−200		−10	−200		V_D = V_S = −10 V	
	INPUT	7	I_{INL}	Input Current Input Voltage Low	−250	−250	−250	−250	−250	−250	µA	V_{IN} = 0	
		8	I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
	DYNAMIC	9	t_{on}	Turn ON Time		250			300		ns	See Switching Time Test Circuit	
		10	t_{off}	Turn-OFF Time		130			150				
		11	$C_{S(off)}$	Source OFF Capacitance	9 Typical*						pF	V_S = −5 V, I_D = 0	f = 1 MHz
		12	$C_{D(off)}$	Drain OFF Capacitance	6 Typical*							V_D = −5 V, I_S = 0	
		13	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14 Typical*							V_D = V_S = 0	
		14		Off Isolation	Typical > 50 dB at 10 MHz							R_L = 75 Ω	

NOTES: 1. V_{IN} = 0.8 V or 2.0 V to turn ON switch under test. 2. V_{IN} = 0.8 V or 2.0 V to turn OFF switch under test.

Monolithic CMOS Analog Switches

Siliconix

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Environmentally Rugged**
  - Latchproof CMOS
- **Low Standby Power**
  - 0.06 μW Typical
- **Minimizes Signal Error**
  - 0.1 nA Typical Leakage
- **Low Operating Power**
  - 0.06 μW Typical for DG304-307
- **Reduced Voltage Drop Across Switch in ON Condition**
  - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
  - Typ t_{on} & $t_{off} < 180$ ns
- **Minimizes System Power Requirements**
  - Single Supply Operation Capabilities
- **Easily Interfaced**
  - TTL, DTL and CMOS Input Compatible
- **Reduces External Component Requirements**
  - Logic Input Overvoltage Protection

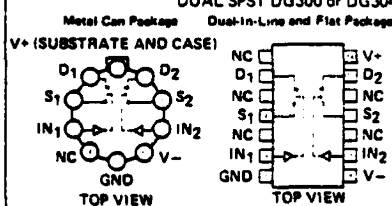
DESCRIPTION

The DG300 through DG307 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, (a few milliwatts for the DG300-303, a few hundred microwatts for the DG304-307), this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The DG300-303 switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The DG304-307 switches are CMOS input compatible and have a logic "0" state with an input less than 3.5 V and a logic "1" state with an input greater than 11 V (for 15 V positive supply). The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG300 or DG304

Metal Can Package — Dual-In-Line and Flat Package



ORDER NUMBERS:
DG300AP OR DG300BP
DG304AP OR DG304BP
SEE PACKAGE 11
DG300CJ
DG304CJ
SEE PACKAGE 7
DG300AL OR DG304AL
SEE PACKAGE 16

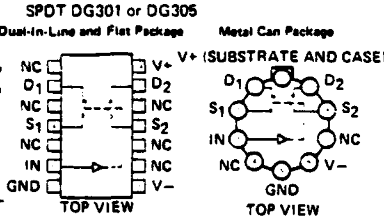
ORDER NUMBERS:
DG300AA OR DG300BA
DG304AA OR DG304BA
SEE PACKAGE 2

LOGIC	SWITCH
0	OFF
1	ON

SPDT DG301 or DG305

Dual-In-Line and Flat Package — Metal Can Package

ORDER NUMBERS:
DG301AP OR DG301BP
DG305AP OR DG305BP
SEE PACKAGE 11
DG301CJ
DG305CJ
SEE PACKAGE 7
DG301AL OR DG305AL
SEE PACKAGE 16

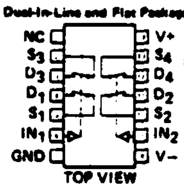


ORDER NUMBERS:
DG301AA OR DG301BA
DG305AA OR DG305BA
SEE PACKAGE 2

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

DUAL DPST DG302 or DG306

Dual-In-Line and Flat Package



ORDER NUMBERS:
DG302AP OR DG302BP
DG306AP OR DG306BP
SEE PACKAGE 11
DG302CJ
DG306CJ
SEE PACKAGE 7
DG302AL OR DG306AL
SEE PACKAGE 16

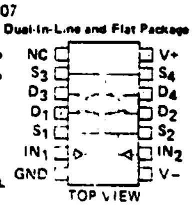
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT DG303 or DG307

LOGIC	SW 1 / SW 2	SW 3 / SW 4
0	OFF	ON
1	ON	OFF

ORDER NUMBERS:
DG303AP OR DG303BP
DG307AP OR DG307BP
SEE PACKAGE 11
DG303CJ
DG307CJ
SEE PACKAGE 7
DG303AL OR DG307AL
SEE PACKAGE 16

Dual-In-Line and Flat Package



SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground	V^+ +18 V, V^+ −36 V
V_S or V_D	V^+ to V^-
V^+ to Ground	+36 V
V^+ to V^-	+36 V
Current, Any Terminal (Except S or D)	30 mA
Current, S or D, Continuous	30 mA
Pulsed 1 ms 10% Duty Cycle	100 mA
Operating Temperature (A Suffix)	−55 to +125°C
(B Suffix)	−20 to +85°C
(C Suffix)	0 to +70°C
Storage Temperature (A & B Suffix)	−65 to +150°C
(C Suffix)	−65 to +125°C

Power Dissipation*	
14 Pin Sidebraze DIP (P)**	825 mW
14 Pin Plastic DIP (J)***	470 mW
Metal Can (A)****	450 mW
Flat Package (L)*****	750 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C
*****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

No.		Characteristics			Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions $V+ = +15$ V, $V- = -15$ V, Gnd = 0 V	
1	SWITCH	V_{ANALOG}	Minimum Analog Signal Handling Capability		±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2		$r_{DS(on)}$	Drain Source ON Resistance		30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
3					30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
4		$I_{S(off)}$	Source OFF Leakage Current		0.1		1	100		5	100	nA	V_S = +14 V, V_D = −14 V	Note 2
5					−0.1		−1	−100		−5	−100		V_S = −14V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current		0.1		1	100		5	100		V_D = +14 V, V_S = −14 V	
7					−0.1		−1	−100		−5	−100		V_D = −14 V, V_S = +14 V	
8		$I_{D(on)}$	Channel ON Leakage Current		0.1		1	100		5	100		$V_D = V_S$ = +14 V	Note 2
9					−0.1		−2	−200		−5	−200		$V_D = V_S$ = −14 V	
10	INPUTS	I_{INH}	Input Current Input Voltage High	DG300-303 Only	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5.0 V	
11				DG300-307 Only	0.001	1*	1	1		1			V_{IN} = +15 V	
12		I_{INL}	Input Current Input Voltage Low		−0.001	−1	−1	−1		−1			V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	DG300-303 Only	150		300					nS	See Switching Time Test Circuit	
14		t_{off}	Turn OFF Time		130		250							
15		t_{on}	Turn ON Time	DG304-307 Only	110		250							
16		t_{off}	Turn OFF Time		70		150							
17		$t_{on} - t_{off}$	Break-Before-Make Interval	DG301/303 DG305/307 Only	50								See Break-Before-Make Time Test Circuit	
18		$C_{S(off)}$	Source OFF Capacitance		14							pF	V_S = 0, Note 2	f = 1 MHz
19		$C_{D(off)}$	Drain OFF Capacitance		14								V_D = 0, Note 2	
20		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		40								$V_D = V_S$ = 0, Note 2	
21		C_{IN}	Input Capacitance		6								V_{IN} = 0	
22					3.5								V_{IN} = +15 V	
23			OFF Isolation[3]		58							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
24	SUPPLY	I+	Positive Supply Current	DG300-303 Only	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
25		I−	Negative Supply Current		−0.001	−10	−10	−100		−100		μA		
26		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0.8 V (All Inputs)	
27		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
28		I+	Positive Supply Current	DG304-307 Only	0.001	10	10	100		100			V_{IN} = +15 V (All Inputs)	
29		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
30		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0 (All Inputs)	
31		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				

NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input voltage to perform proper function. DG300-303: V_{IN} – For logic "1" = 4 V, for logic "0" = 0.8 V. DG304-307: V_{IN} – For logic "1" = 11 V, for logic "0" = 3.5 V
3. "OFF" Isolation = 20 log V_S/V_D, V_S = Input to OFF switch, V_D = Output. Since the DG300-301 and DG304/305 have a N/C pin between S and D, the OFF Isolation generally improves by 7 dB @ 500 KHz over value shown here.

DG300 ICMA-A	DG302 ICMB-A
DG301 ICMA-B	DG303 ICMB-B
DG304 ICMA-C	DG306 ICMB-C
DG305 ICMA-D	DG307 ICMB-D

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as SN52709/SN72709

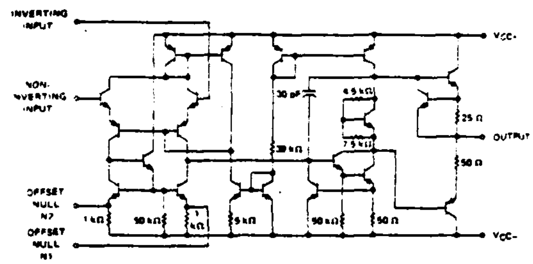
description

The SN52741 and SN72741 are high-performance operational amplifiers, featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

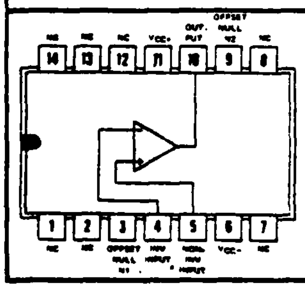
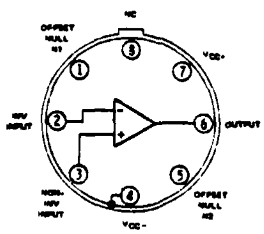
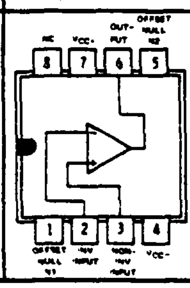
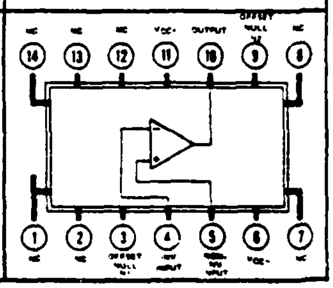
The SN52741 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72741 is characterized for operation from 0°C to 70°C.

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)	Z FLAT PACKAGE (TOP VIEW)
	 PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE		

NC—No internal connection

1170

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN52741	SN72741	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 55°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or Z Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the SN52741 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 55°C free-air temperature, refer to Dissipation Derating Curve, Figure 12.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		SN52741 MIN	SN52741 TYP	SN52741 MAX	SN72741 MIN	SN72741 TYP	SN72741 MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	25°C	24	28		24	28		V
		$R_L \geq 10$ kΩ	Full range	24			24			
		$R_L = 2$ kΩ	25°C	20	26		20	26		
		$R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ,	25°C	50,000	200,000		20,000	200,000		
		$V_O = \pm 10$ V	Full range	25,000			15,000			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$ V, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load,	25°C		1.7	2.8		1.7	2.8	mA
		No signal	Full range			3.3			3.3	
P_D	Total power dissipation	No load,	25°C		50	85		50	85	mW
		No signal	Full range			100			100	

†All characteristics are specified under open-loop operation. Full range for SN52741 is −55°C to 125°C and for SN72741 is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

VITA

Dundar Satirtav was born the son of Celil and Sacide Satirtav on 20 February 1957 in Tire, Izmir, Turkey. He graduated from the Air Force Senior High School in Izmir, and entered the Turkish Air Force Academy in 1974. He received the degree Bachelor of Science in Electrical Engineering, and was commissioned as a second lieutenant on 30 August 1978. He attended the Air Force Communication School for a year and was assigned to Murted Air Force Base in Ankara, where he served as communication officer. He entered the School of Engineering, Air Force Institute of Technology in June 1981.

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In the literature, there are many technical papers describing the theoretical characteristics, advantages and disadvantages of switched-capacitor circuits and systems. The experimental research presented here is an investigation of the characteristics of specific switched-capacitor circuits as described by some of these technical papers. The circuits investigated include a second order band elimination filter, a simulation of inductor and a AM demodulator. For each circuit, the performance of the switched-capacitor implementation was compared to the theoretical analysis. In addition, for the band elimination filter and inductor circuits, the performance of the switched-capacitor circuit was compared to an equivalent implementation using normal analog components. Analatical results were duplicated using switched-capacitor circuits. The clock frequency was a critical parameter for the experiment.

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